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MS-7B49

ATX
Ver: 1.0

Intel -Coffeelake plamform Z370

CPU:

Coffeelake-S

System Chipset:

Z370

Onboard Chip:

HD Audio Codec : ALC887

LAN : Intel I219

SIO : Nuvoton 6795

Flash ROM : 16MB GSE Z270
8MB GSE Lite For H270 / B250

Main Memory:

DDRIV (800/1066/1333/1600/2133MHz) * 4 (Dual Channel)

ACPI:

NIKO/UPI

PWM:

UP9508

Expansion Slots:

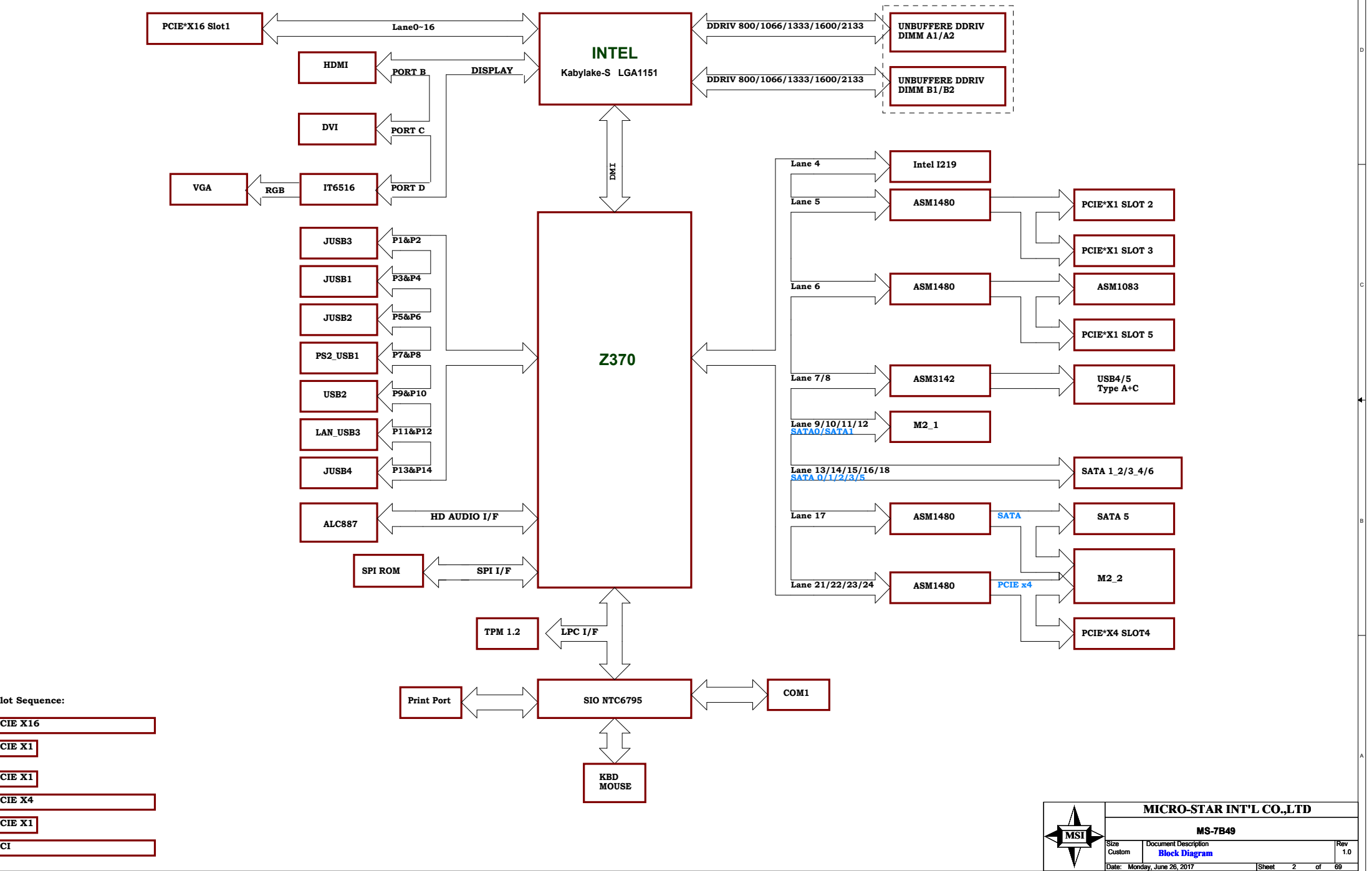
PCI Express (X16) Slot *1
PCI Express (X4) Slot * 1
PCI Express (X1) Slot * 3
PCI Slot * 1
M2 * 2 (22110 and 2280)

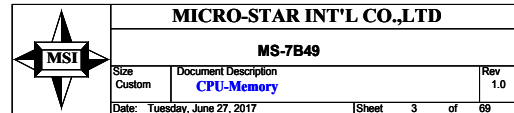
Other:

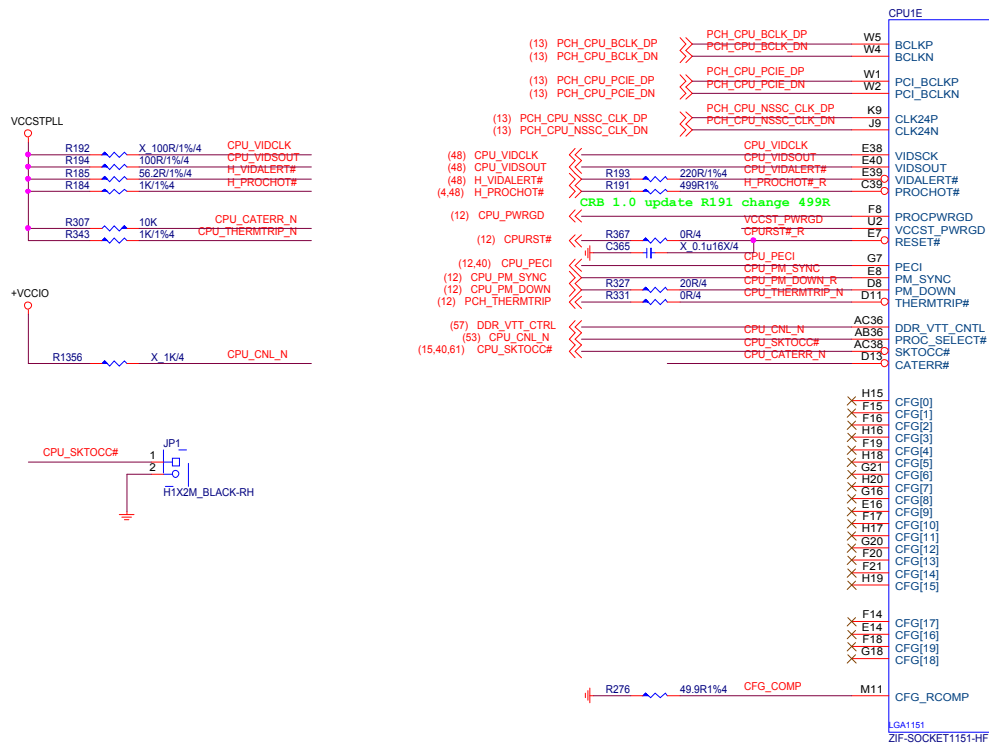
SATA3.0 x6 (PCH)
FRONT USB2.0 *4
FRONT USB3.0 *4(B250 only 2)
REAR USB2.0 *2
REAR USB3.0 *4
REAR USB3.1 TYPE A+C

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MS-7B49 Block Diagram

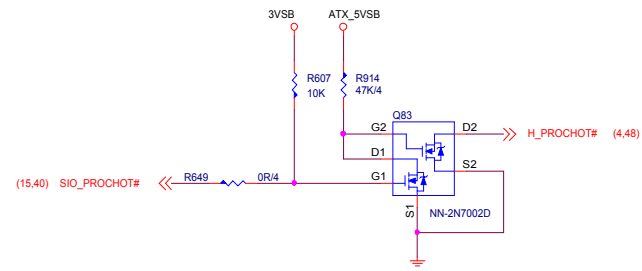
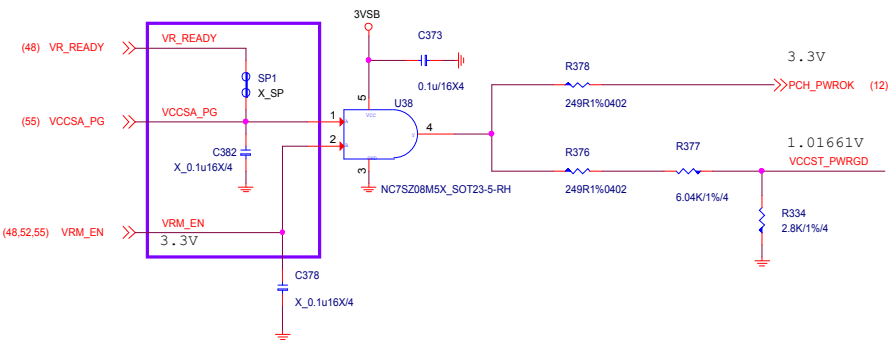
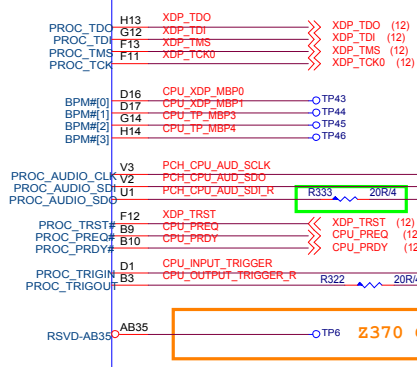
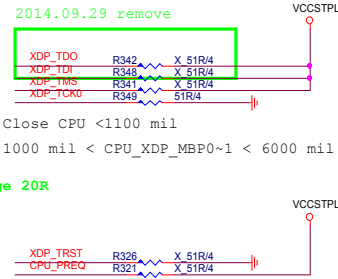


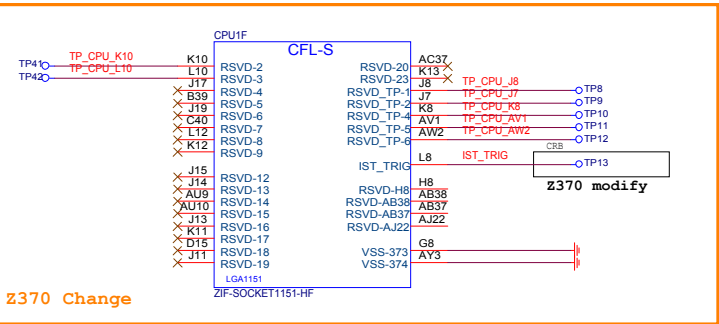
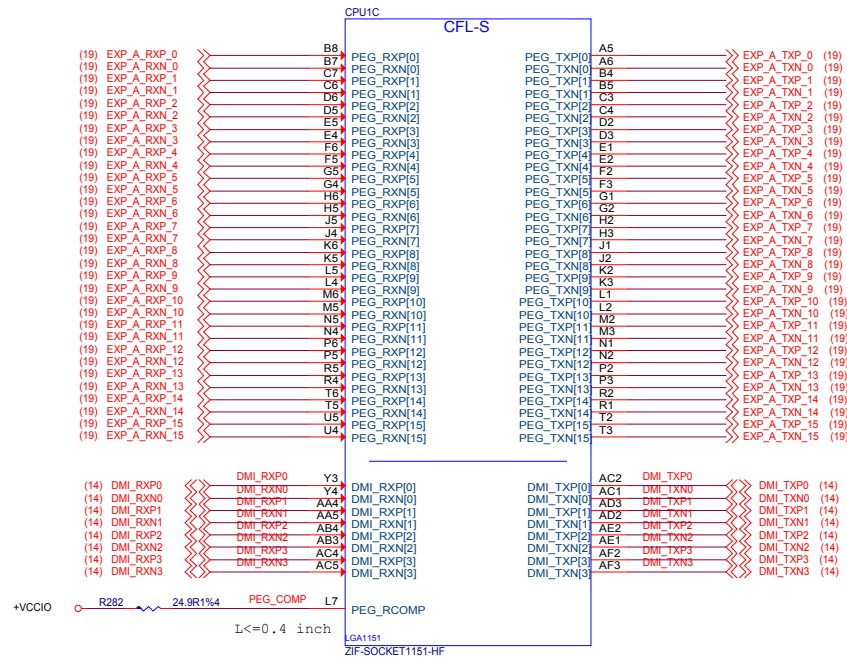




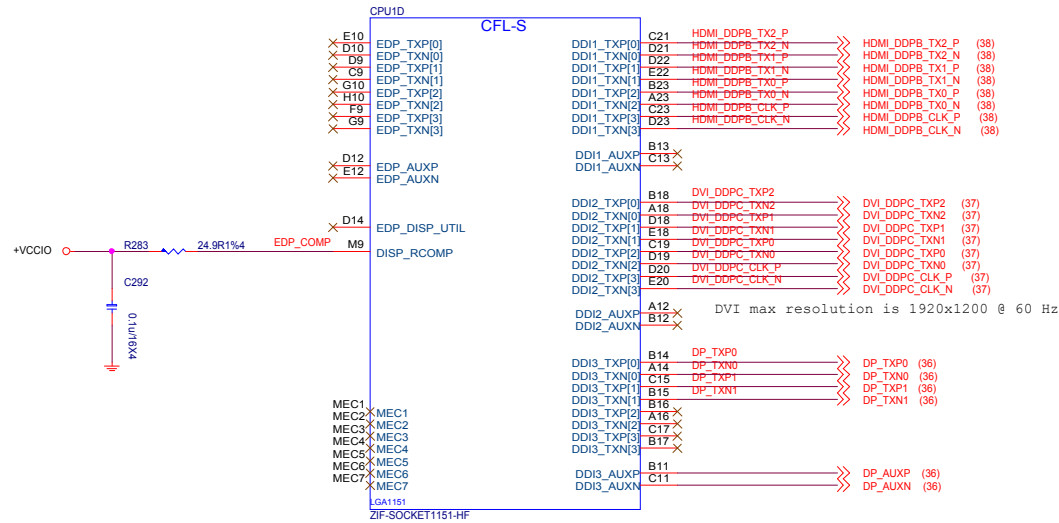
CFG Strap			
CFG Table			
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL Lock
1			RSVD
2	NORM	REVERSE	PEG LAKE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8			RSVD
9	PRESENT	NO PRESENT	SVID PRESENT
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		RSVD
15	RSVD		RSVD

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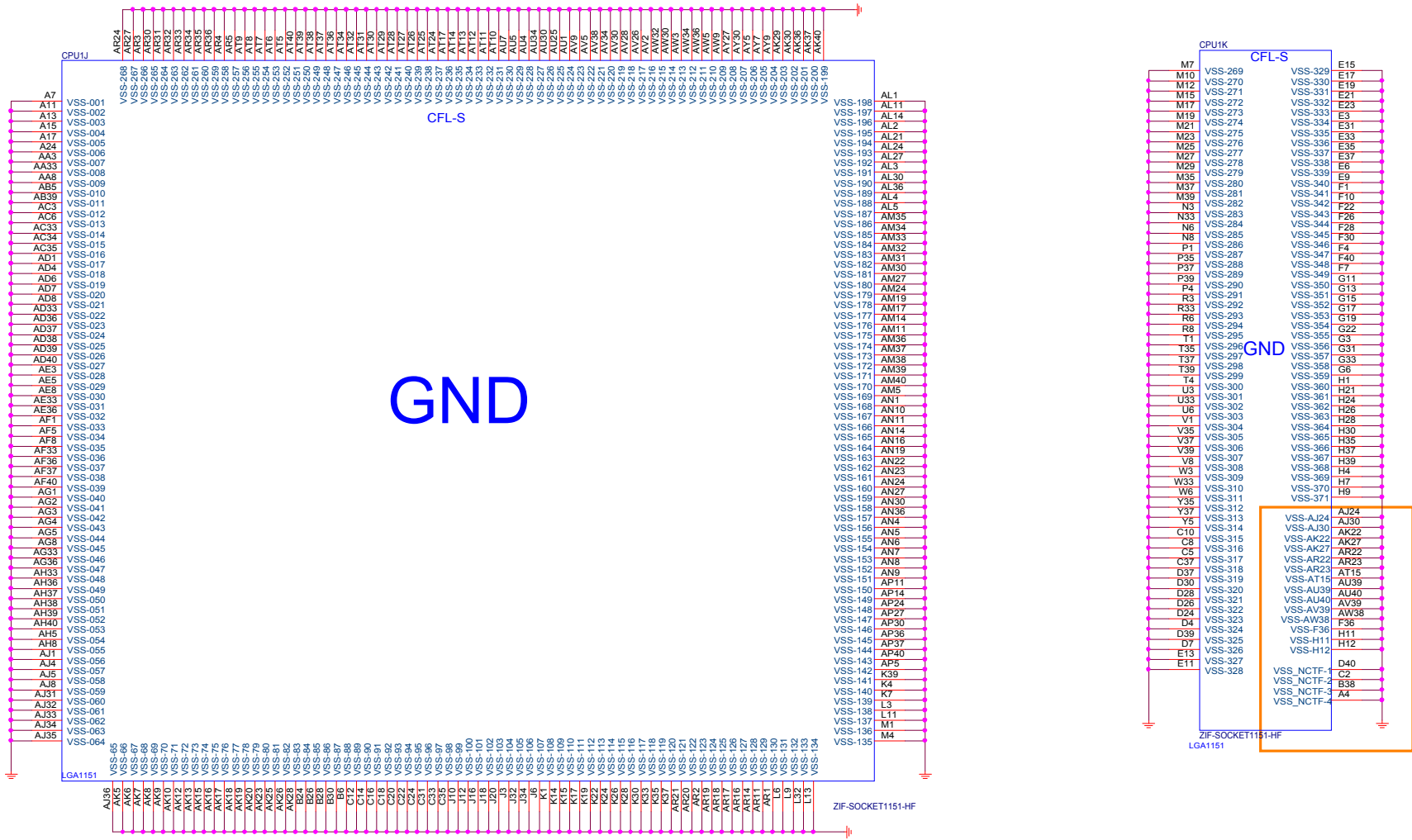


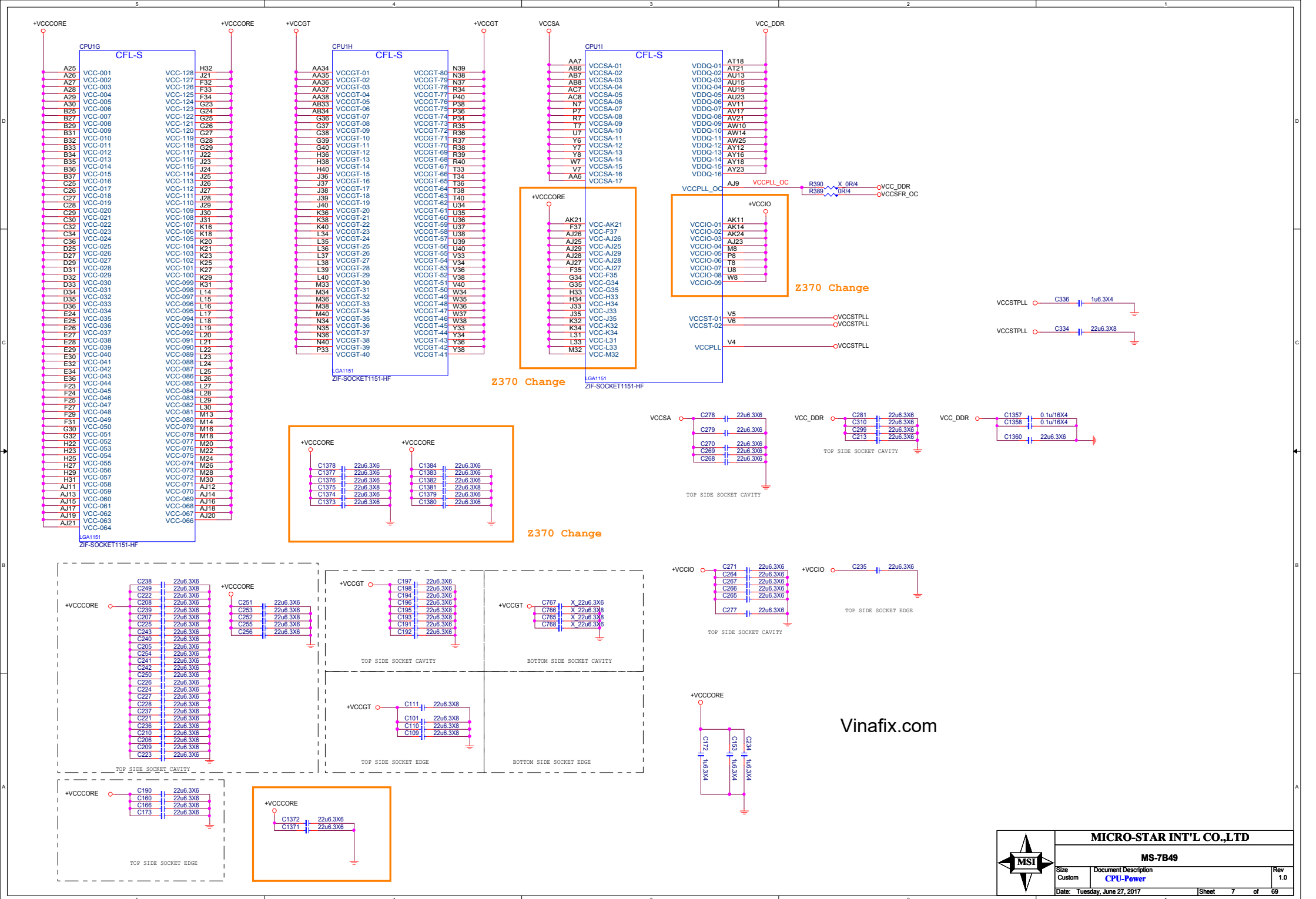


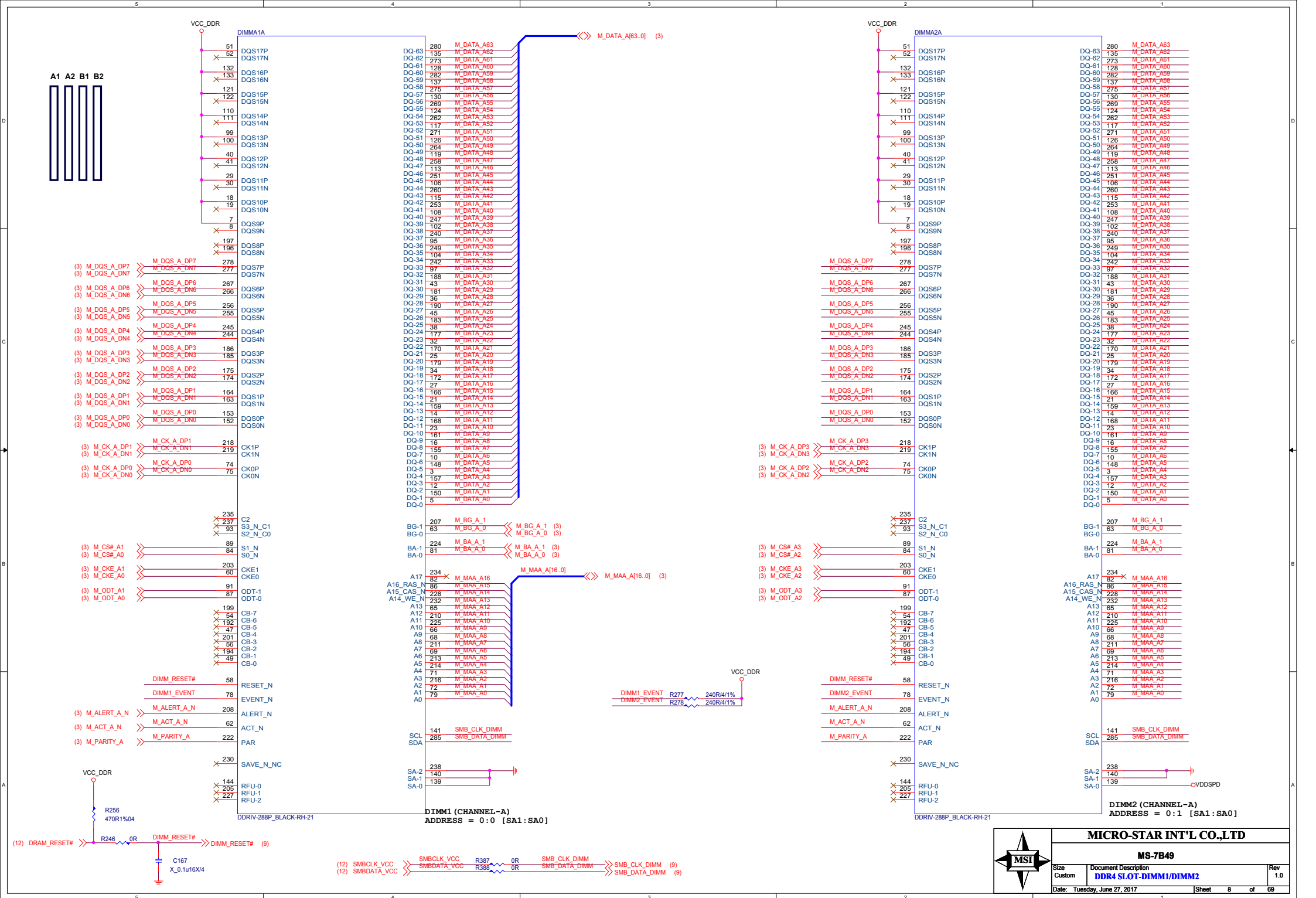
TP8, TP9, TP10, TP11, TP12, TP13, TP41, TP42
Reservd for CPU XDP debug pin

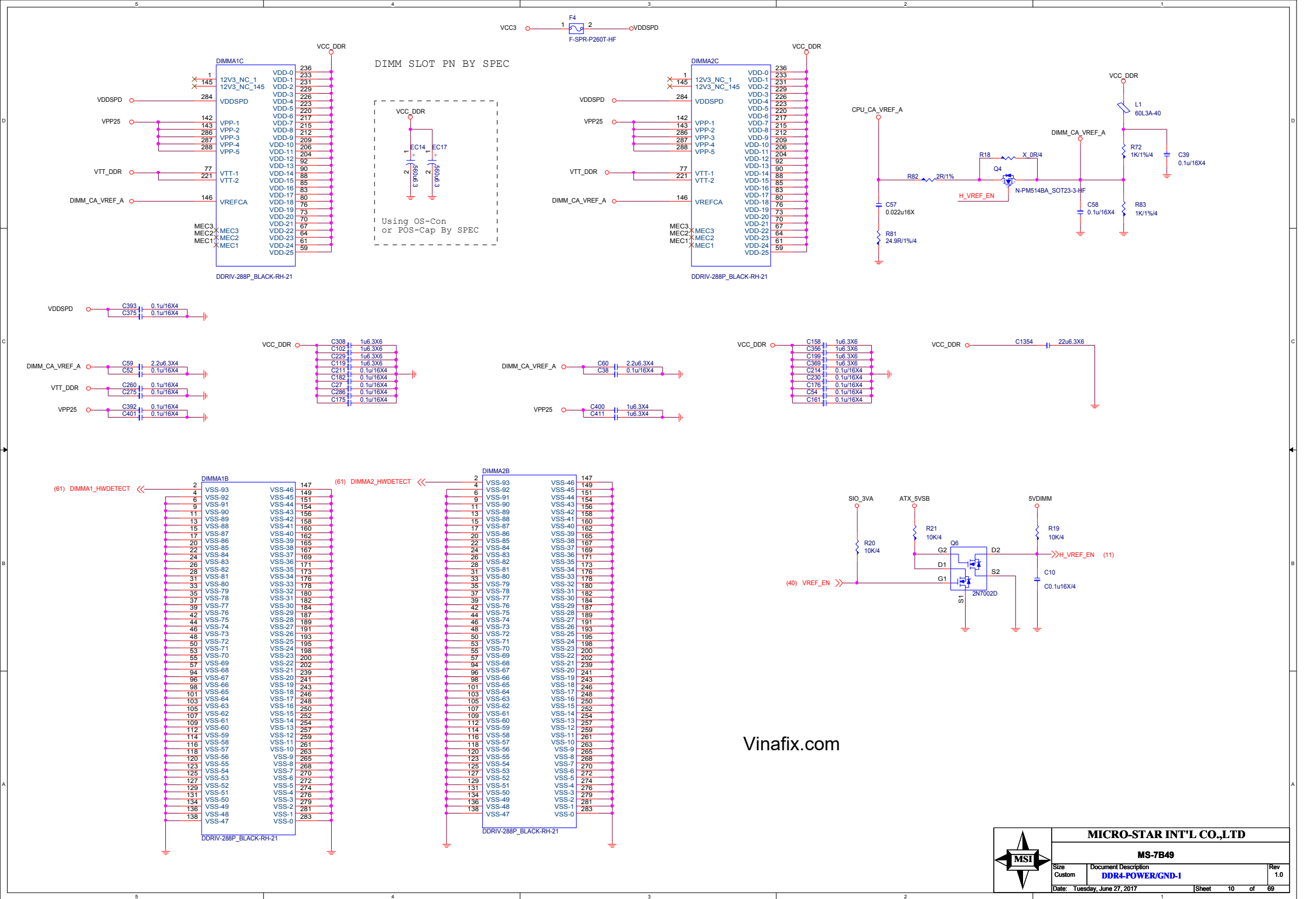


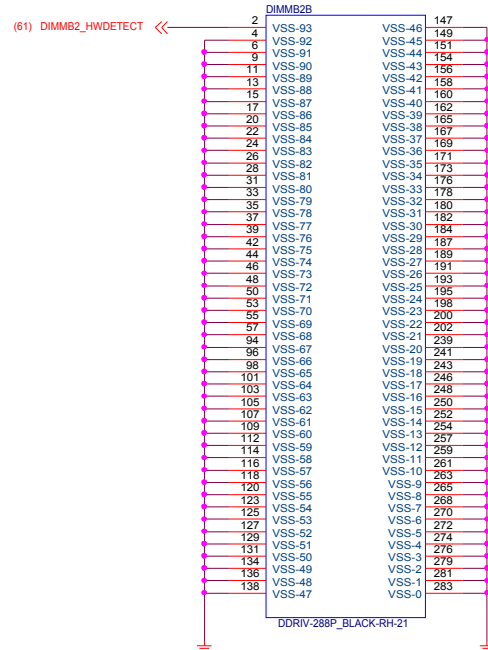
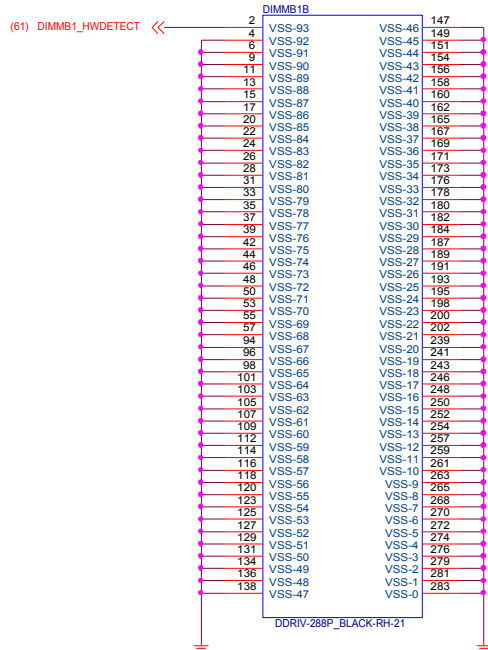
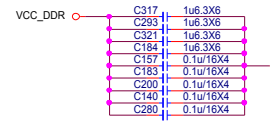
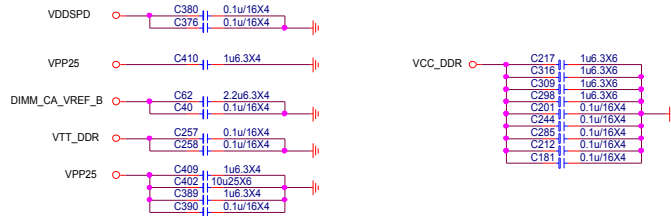
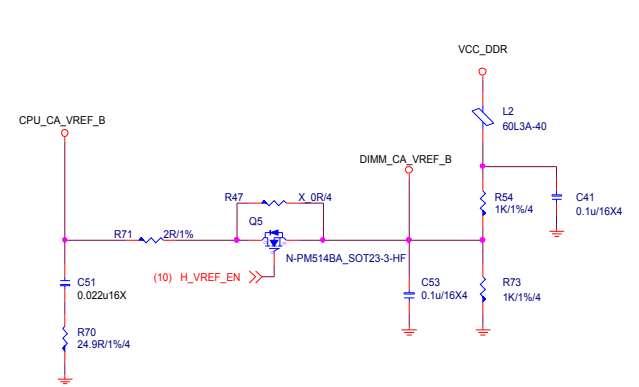
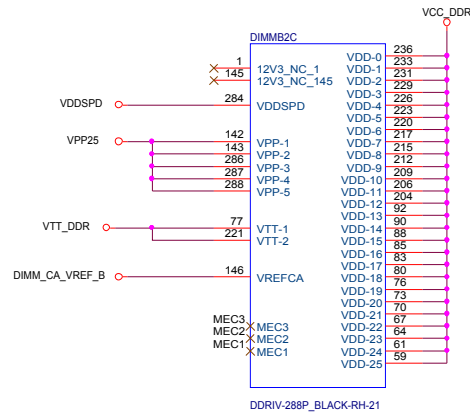
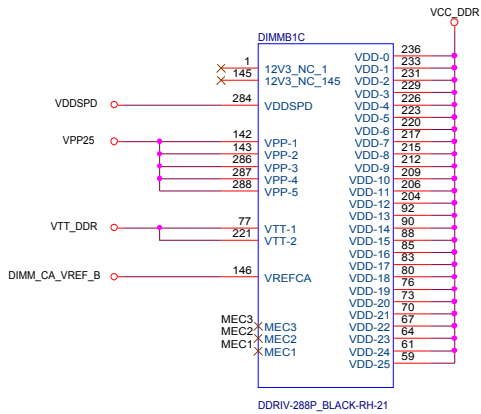
Vinafix.com

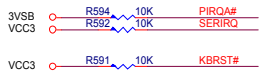




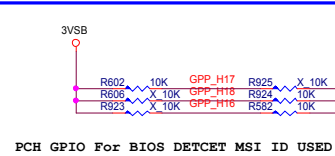
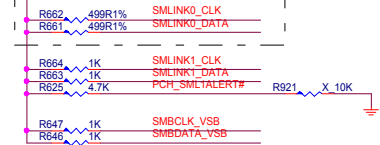




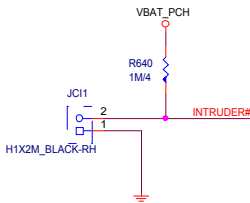




LANPHY USE by SPEC

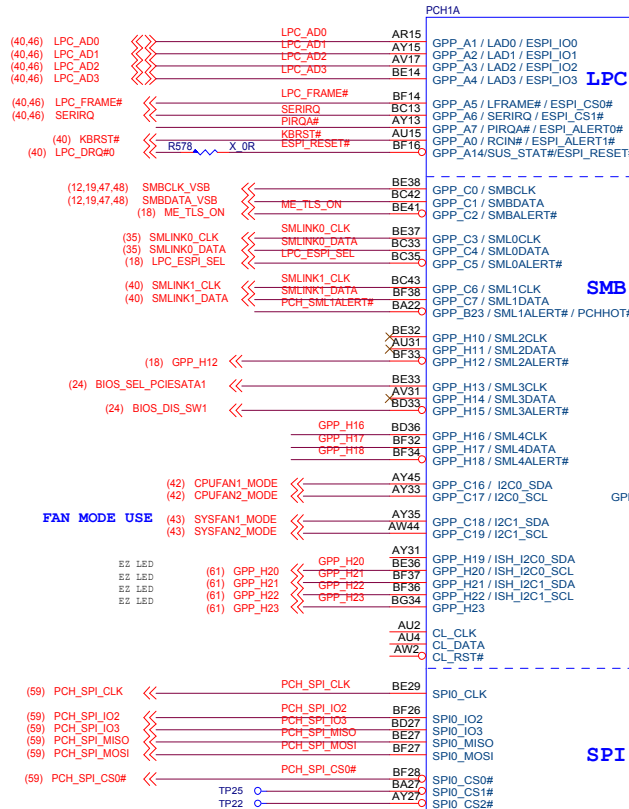
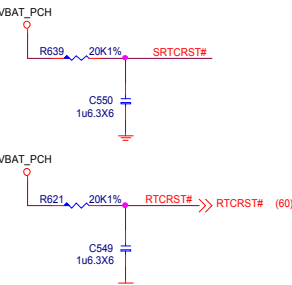


Chassis Intrusion



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RTC



Power Management

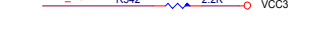
STRAP

SPI JTAG

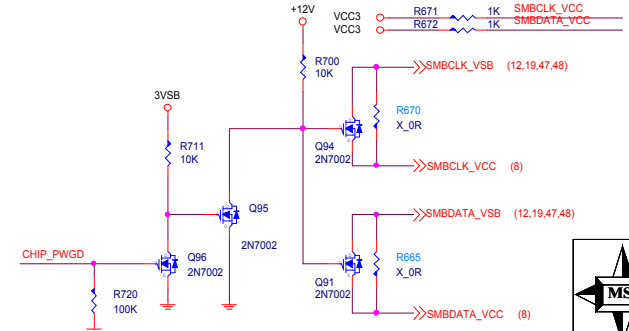


PCH LANPHY PWR

Pull Down PCH PHY into low power state.
For No Use intel Lan



擺在一起 (注意到所有的SMBUS的分枝)

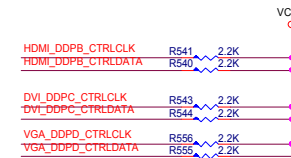
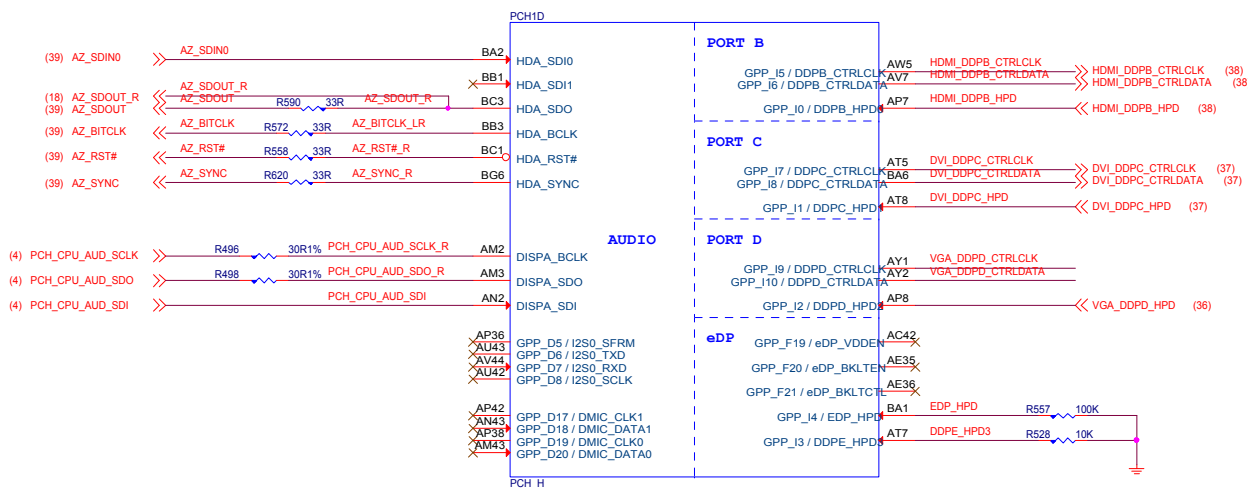
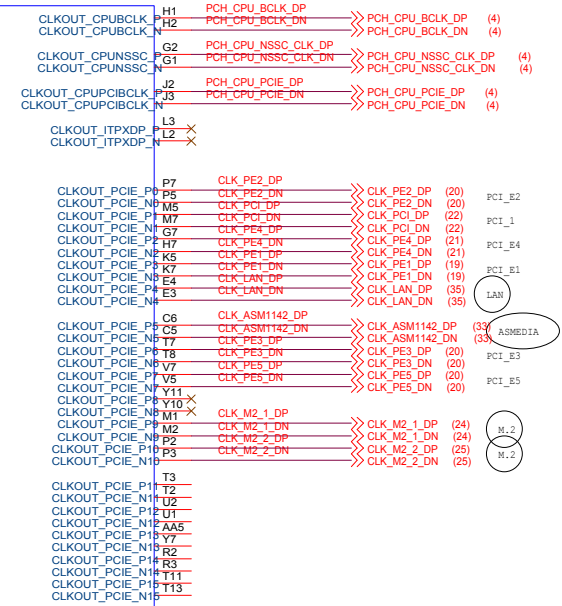
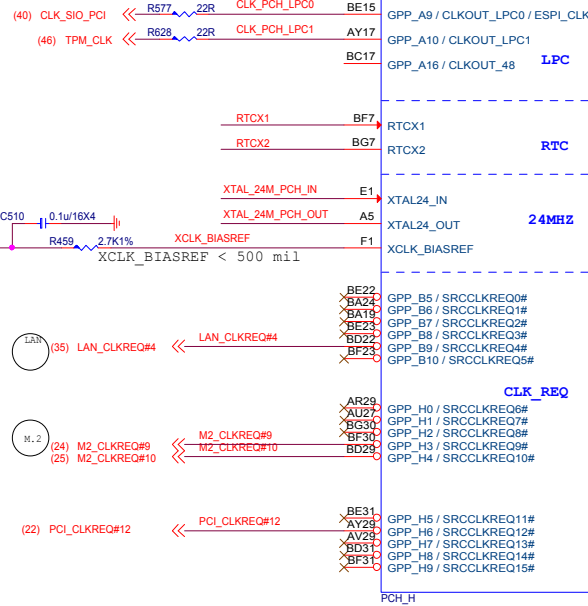
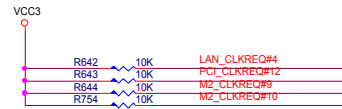
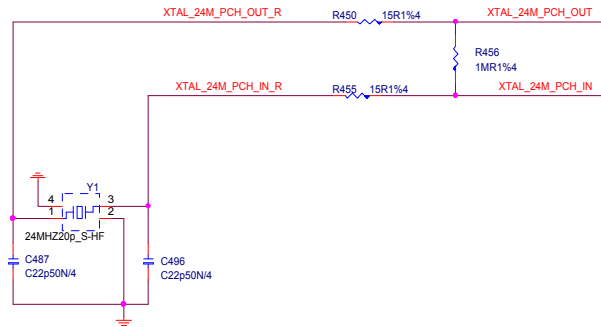
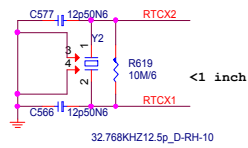


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PCH_CLK

RTC Block

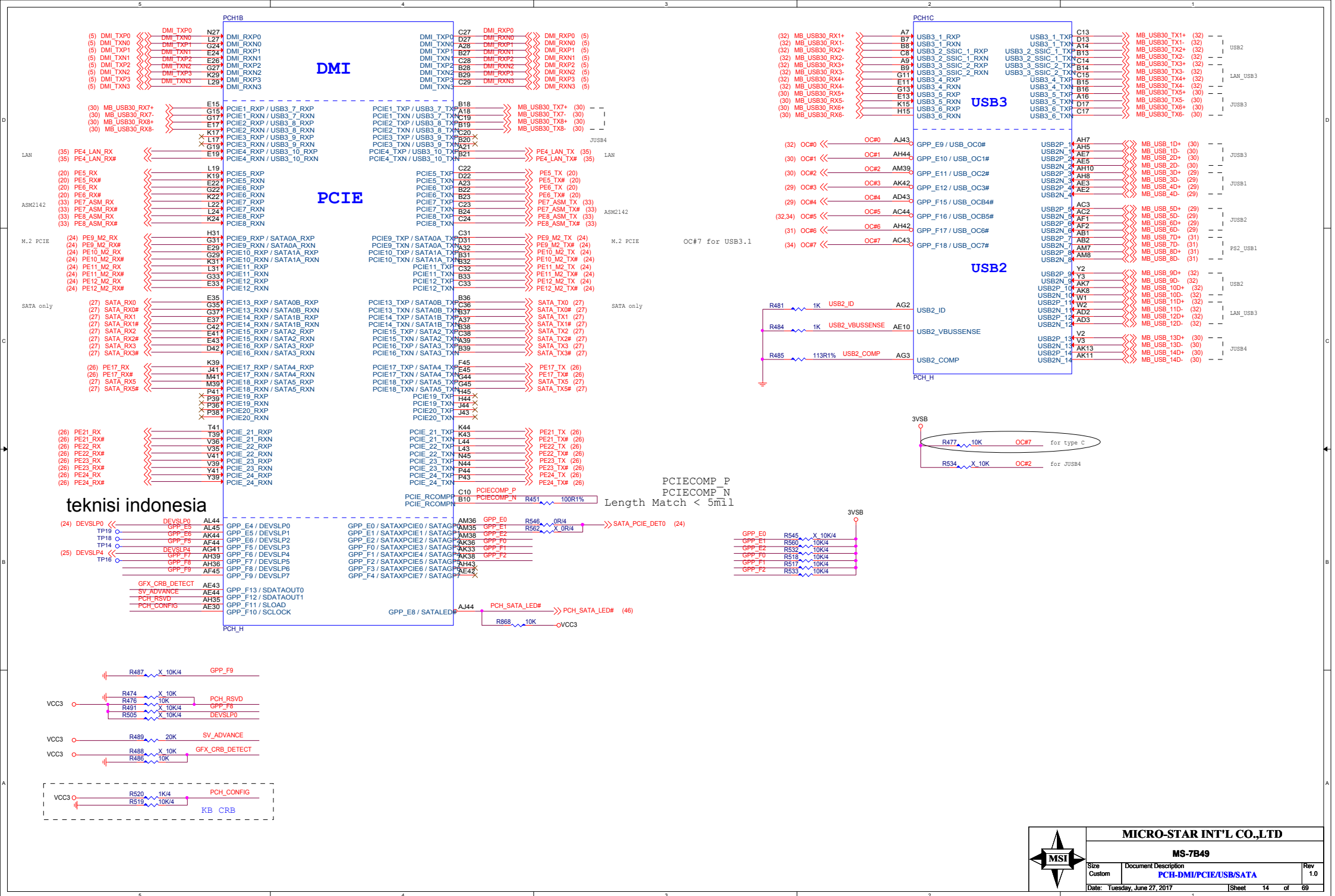
Close to PCH



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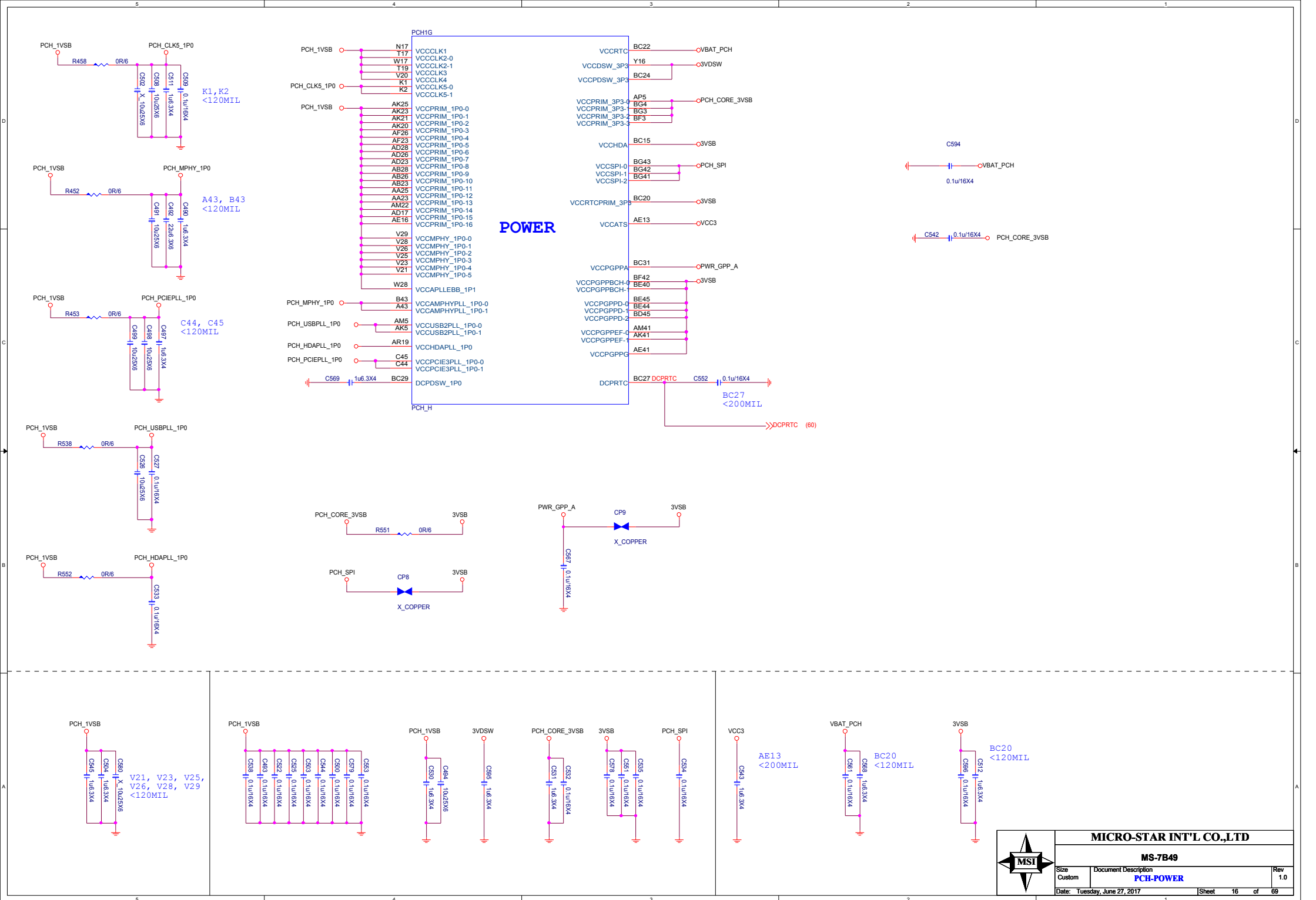
MS-7B49

Size Custom	Document Description PCH-Clock/Audio	Rev 1.0
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PCIECOMP_P
PCIECOMP_N
Length Match < 5mil



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VSS

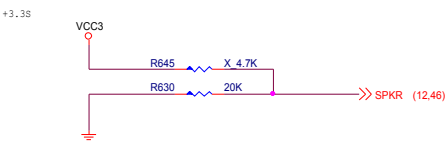


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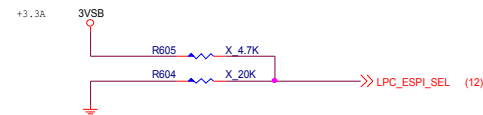
Size	Document Description	Rev
Custom	PCH-GND	1.0
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TOP Swap



Internal pull-down is disabled after PLTRST#

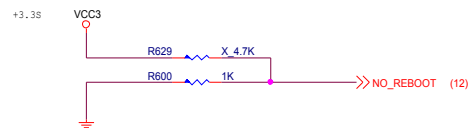
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down is disabled after RSMRST

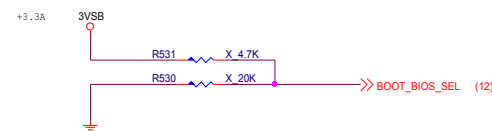
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down is disabled after PLTRST#

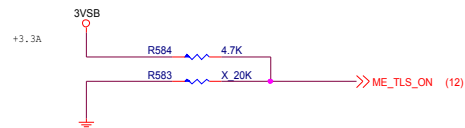
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down is disabled after PLTRST

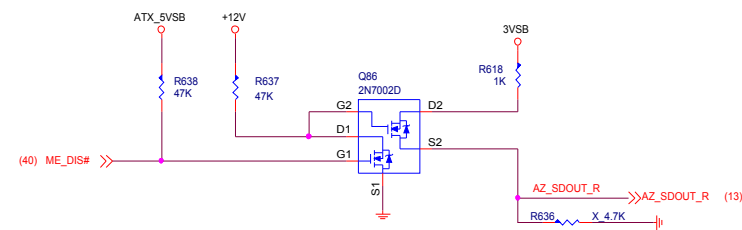
AMT and SBA with confidentiality



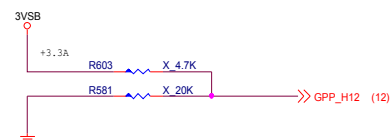
0 : DISABLE
1 : ENABLE (Default)

Internal pull-down is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE



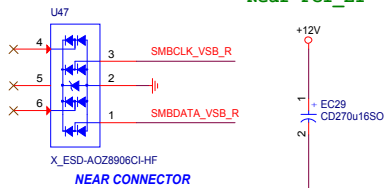
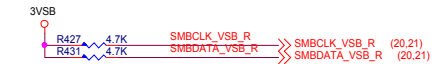
0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down is disabled after RSMRST

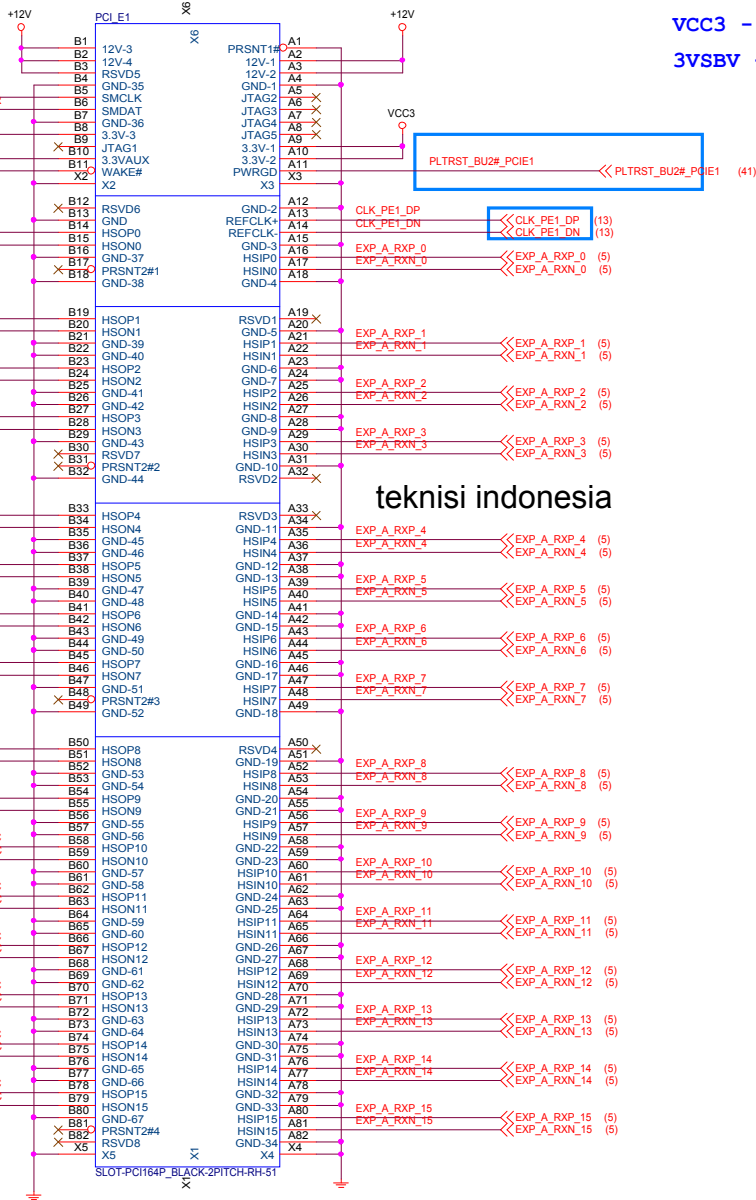
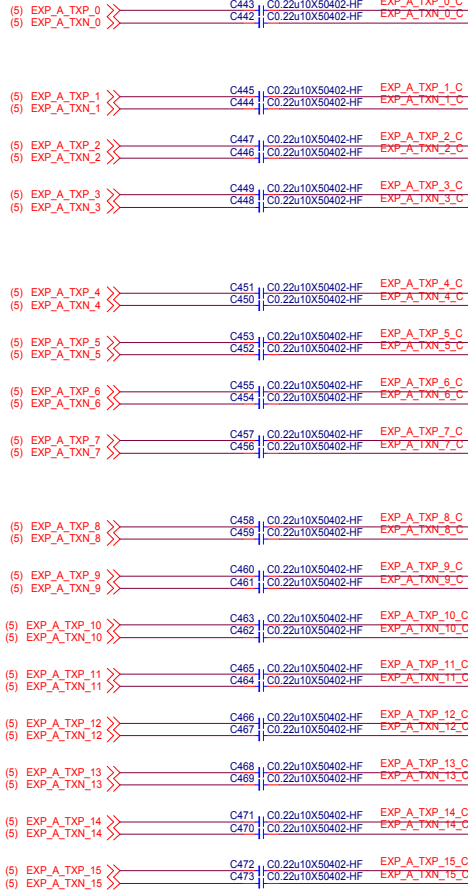


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12V - 5.5A
VCC3 - 3A
3VSB - 375mA



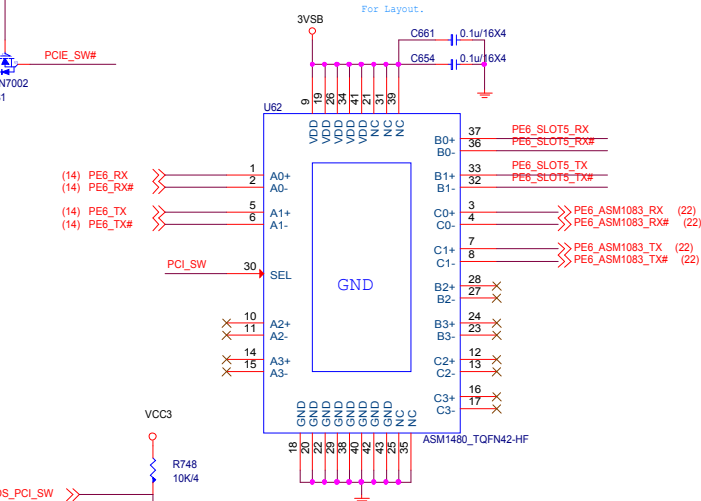
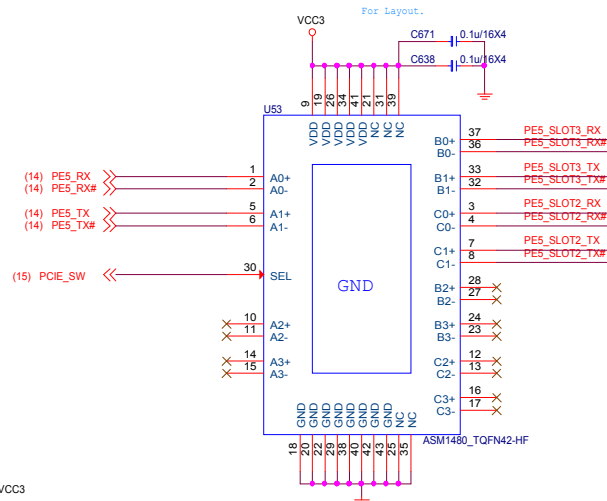
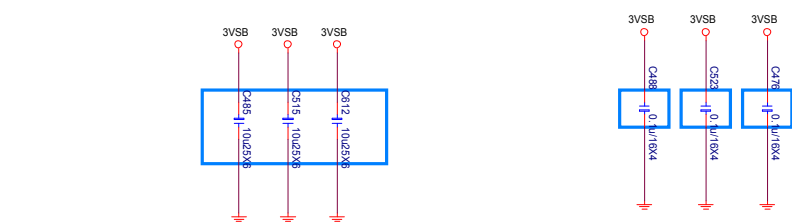
(12,20,21,24,25,33) SB_WAKE# <<<



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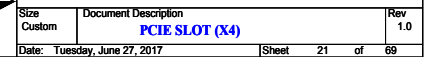
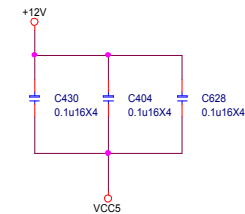
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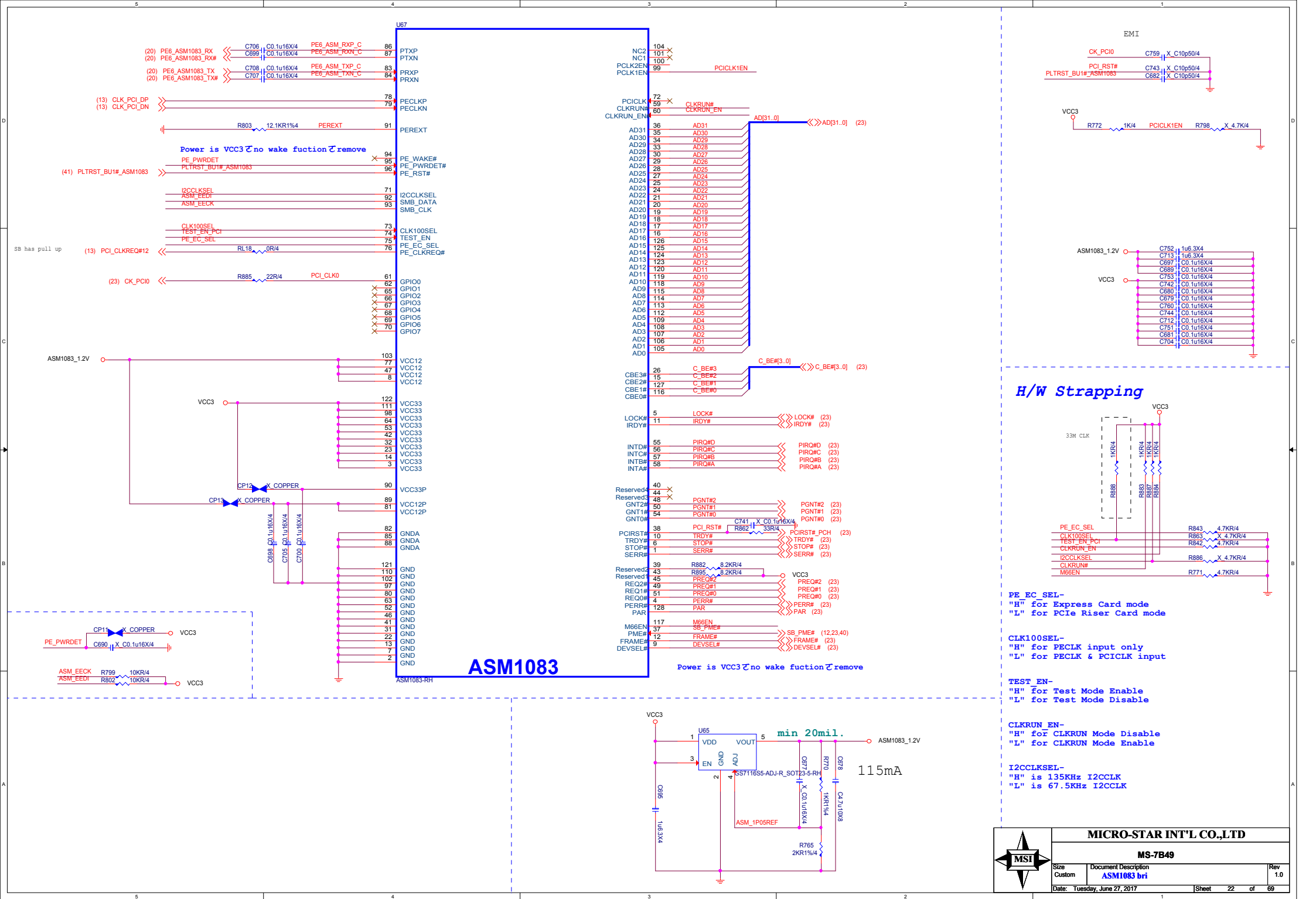


MS-7B49

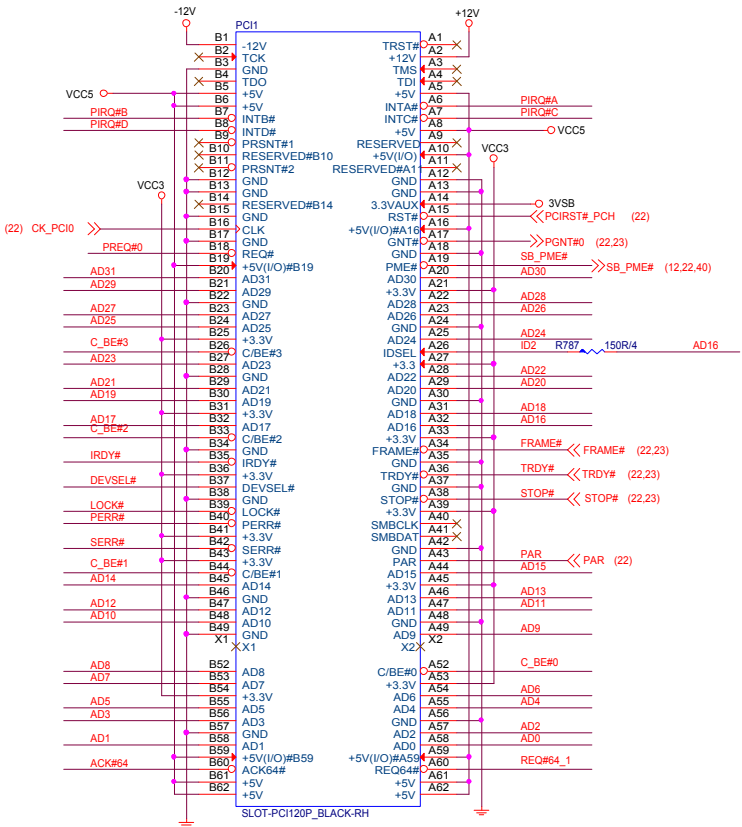
Size Custom	Document Description PCIE SLOT (X1)	Rev 1.0
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12V - 2.1A
VCC3 - 3A
3VSBV - 375mA

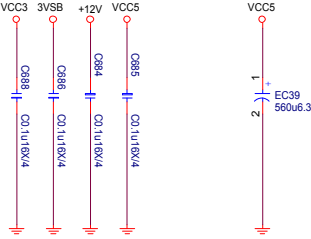





```
3.3Vaux:0.375*2=0.75A(wake)
0.02*2=0.04A(no wake)
VCC3 :7.6*2=15.2A
VCC5:5*2=10A
+12V:0.5*2=1A
-12V:0.1*2=0.2A
```



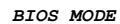
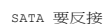
```
EMI:close pin
```



Signal	Function	Pin	Level
(22) DEVEL#	DEVEL#	R791	8.2KRU/4
(22,23) TRDY#	TRDY#	R790	8.2KRU/4
(22) IRDY#	IRDY#	R789	8.2KRU/4
(22,23) FRAME#	FRAME#	R788	8.2KRU/4
(22) SERR#	SERR#	R795	8.2KRU/4
(22) PERR#	PERR#	R794	8.2KRU/4
(22) LOCK#	LOCK#	R793	8.2KRU/4
(22,23) STOP#	STOP#	R792	8.2KRU/4
(22) PREQ#2	PREQ#2	R896	X 8.2KRU/4
(22) PREQ#1	PREQ#1	R898	X 8.2KRU/4
(22) PREQ#0	PREQ#0	R824	X 8.2KRU/4
(22) PGMT#2	PGMT#2	R887	X 8.2KRU/4
(22) PGMT#1	PGMT#1	R889	X 8.2KRU/4
(22,23) PGMT#0	PGMT#0	R825	8.2KRU/4
(22) PIRO#D	PIRO#D	R824	8.2KRU/4
(22) PIRO#C	PIRO#C	R822	8.2KRU/4
(22) PIRO#B	PIRO#B	R831	8.2KRU/4
(22) PIRO#A	PIRO#A	R830	8.2KRU/4
	ACK#64	R796	8.2KRU/4
	REQ#64_1	R797	8.2KRU/4



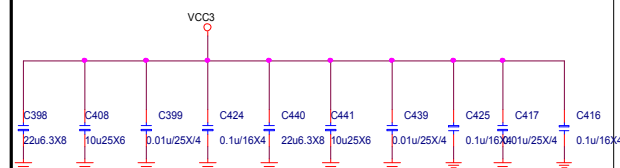
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Footprint: H R240D173 BR189 PT



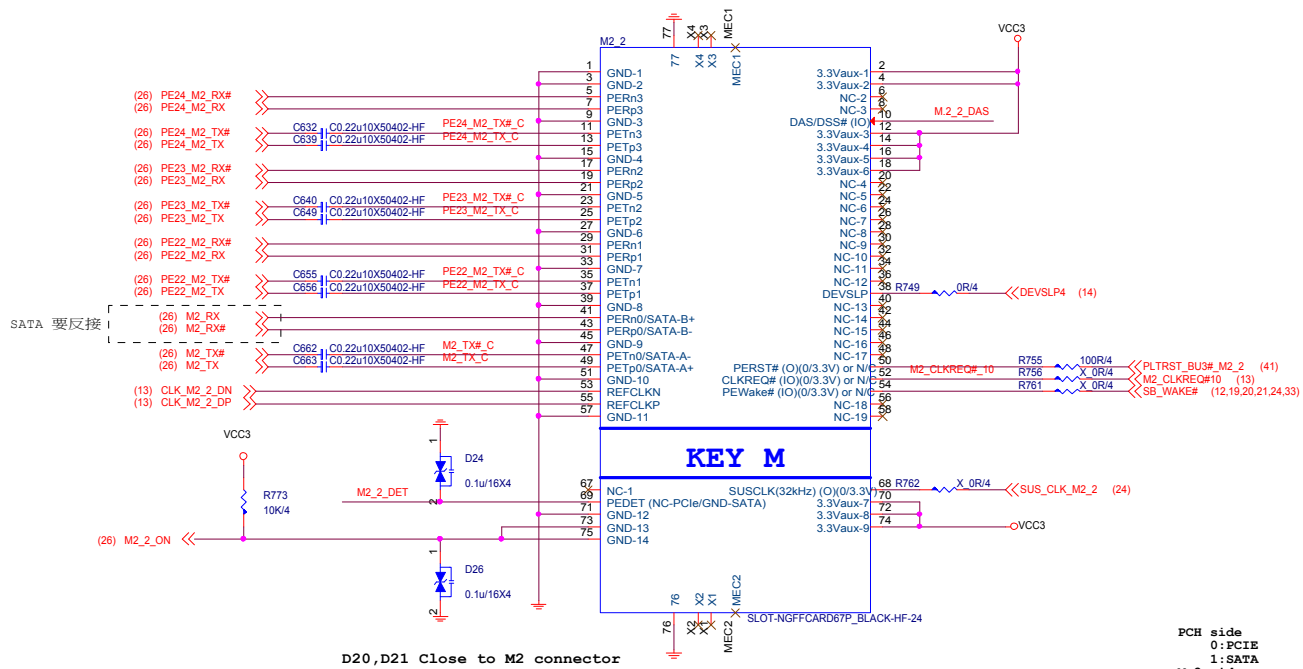
M:E2B-7B05020-A89
S:E2B-7B05020-H75



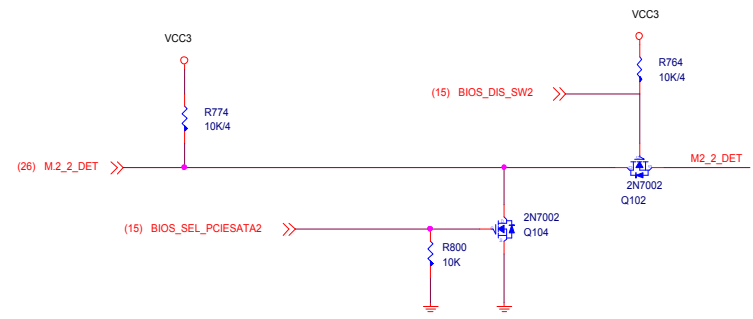
MICRO-STAR INT'L CO.,LTD

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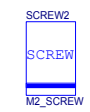


PCH side
0:PCIE
1:SATA
M.2 side
0:SATA
NC:PCIE

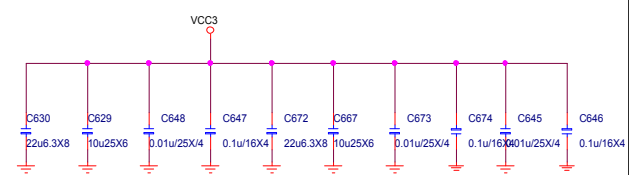



BIOS_MODE		
BIOS_DIS_SW2	BIOS_SEL_PCIESATA2	Mode
1	0	M2-PCIE
0	1	X4 SLOL-PCIE
GPI	GPI	GPI

M:E2B-7B05020-A89
S:E2B-7B05020-H75



Footprint: H_R240D173_BR189_PT

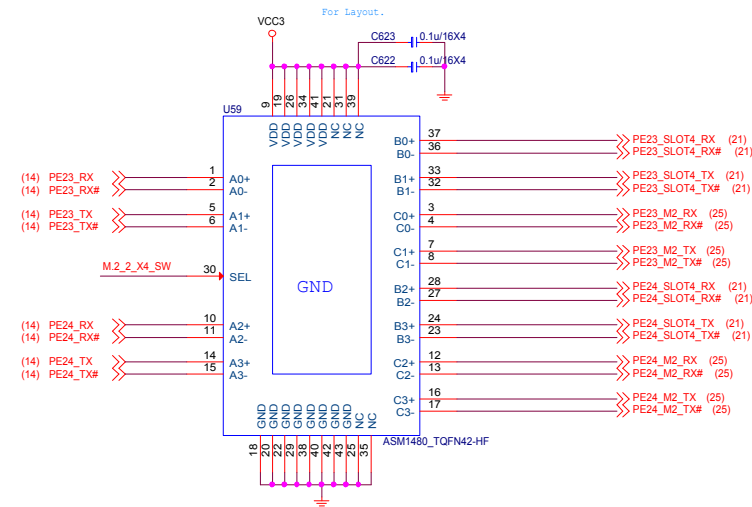
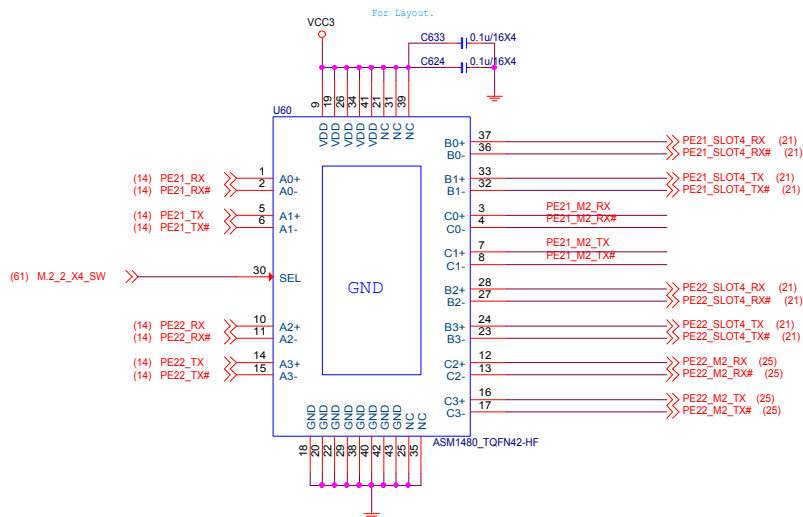
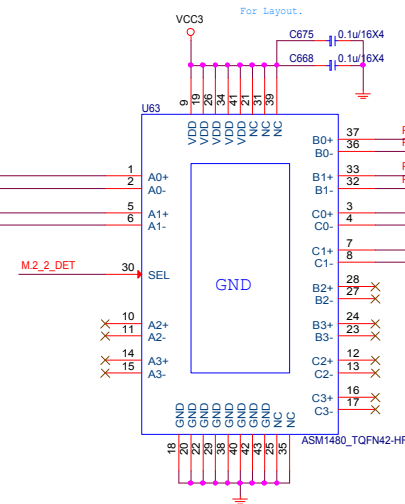
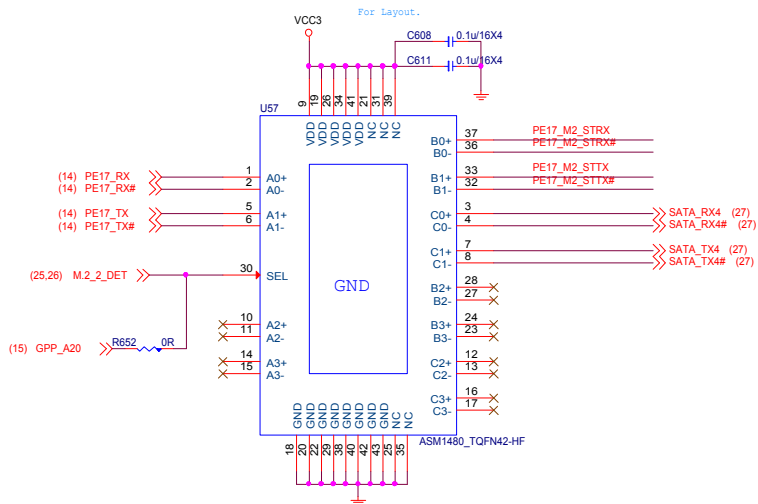




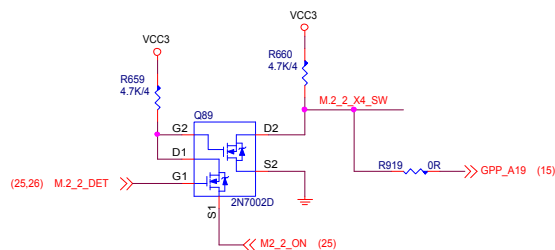
MICRO-STAR INT'L CO.,LTD

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Custom	M2-SLOT2	1.0
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Default

M.2_2 PCIE

M.2_2 SATA

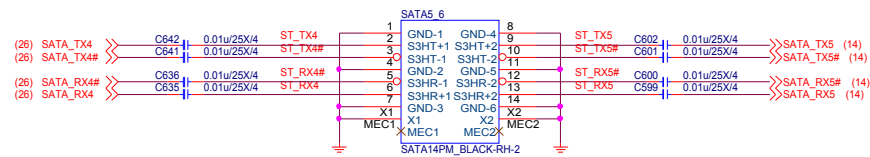
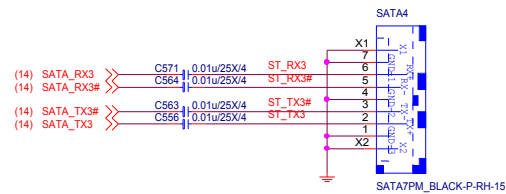
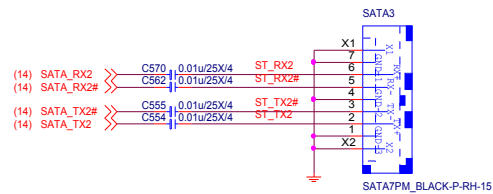
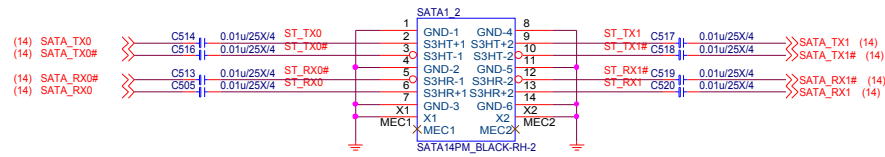
M.2_2_ON	M.2_2_X4_SW	M.2 SATA	M.2 PCIE	X4 SLOT	SATA5
V	V	X	X	V	V
X	X	X	V	X	V
X	V	V	X	V	X



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Custom	M.2/SATA/PCIE SW	1.0
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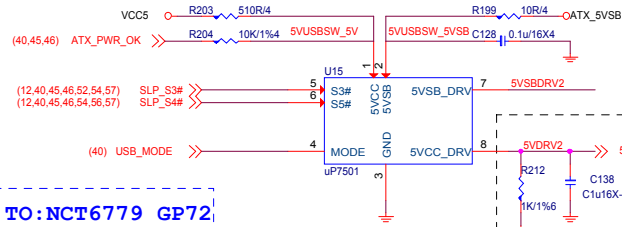


MICRO-STAR INT'L CO.,LTD

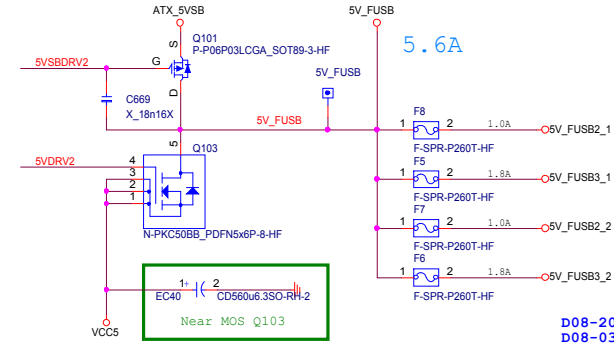
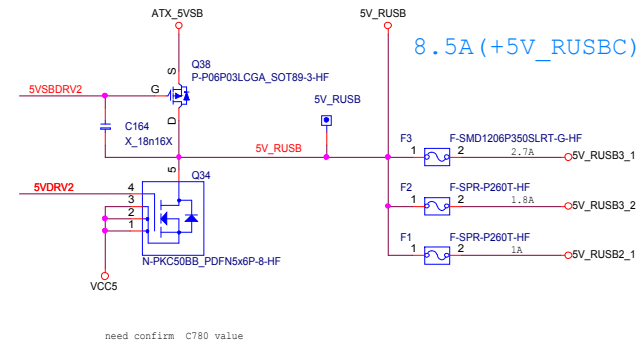
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Size	Document Description	Rev
Custom	SATA Express/SATA Connector	1.0
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REAR USB PORT POWER



5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.



P-MOS
D03-06P0319-N03

N-MOS
D03-510BA0C-N03
D03-3056M00-U47
D03-4C05N03-O05
D03-3830D09-N47
D03-632BA0C-N03

D08-2000400-P16 (Itrip=3.5A; 0.003ohm)
D08-0301000-P16 (Itrip=2.6A; 0.015ohm)

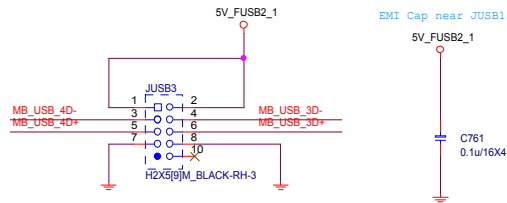
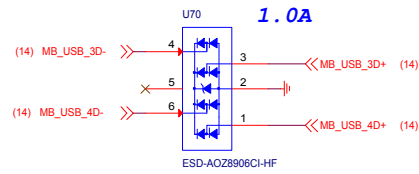
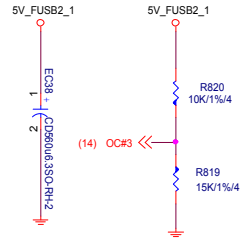
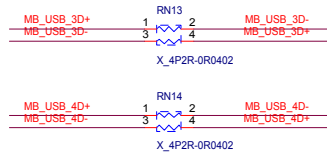


MICRO-STAR INT'L CO.,LTD

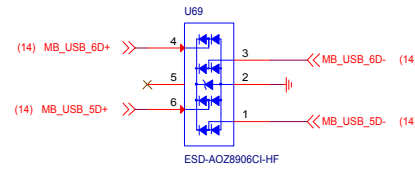
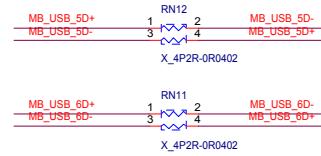
MS-7B49

Size	Document Description	Rev
Custom	USB POWER-MP149S/UP7501	1.0
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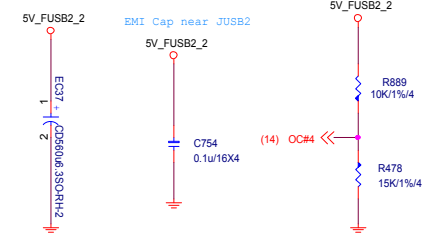
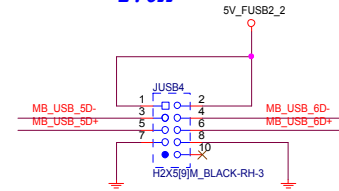
FRONT USB2.0 PORT 3,4



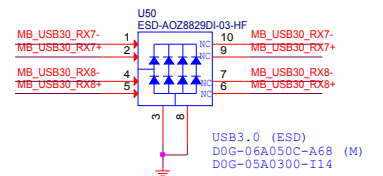
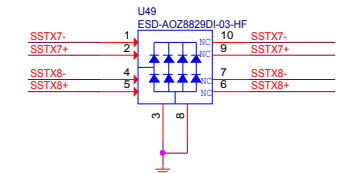
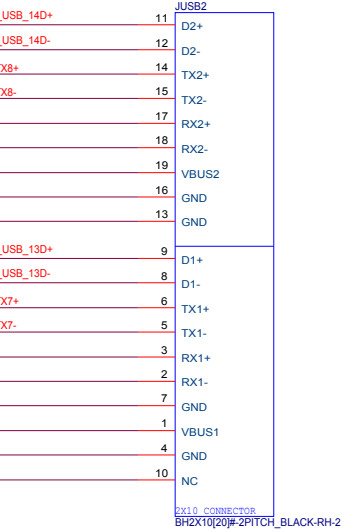
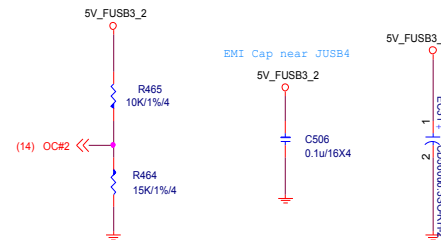
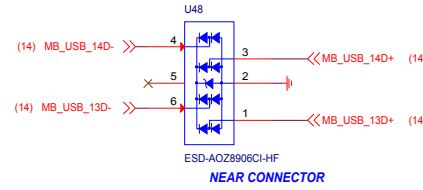
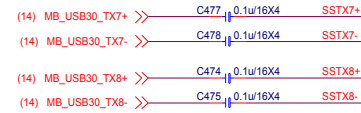
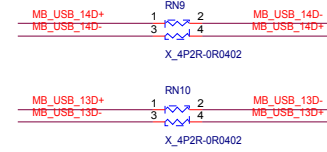
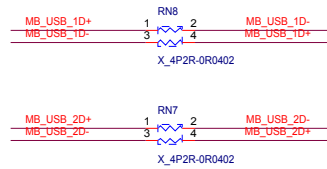
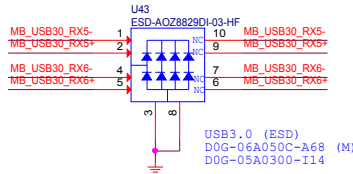
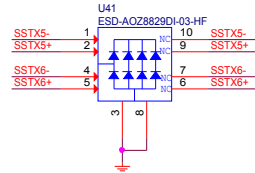
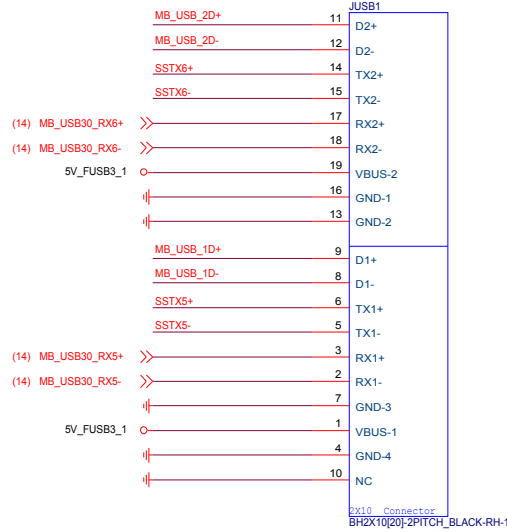
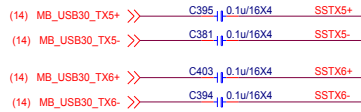
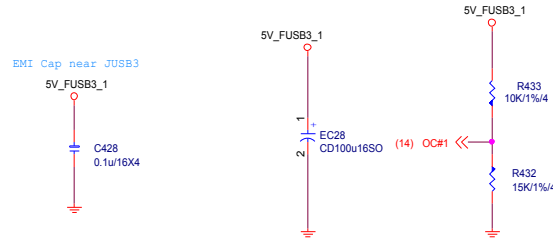
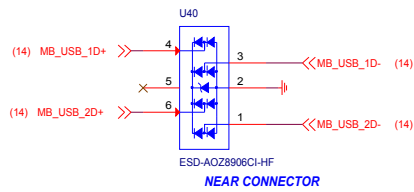
FRONT USB2.0 PORT 5,6



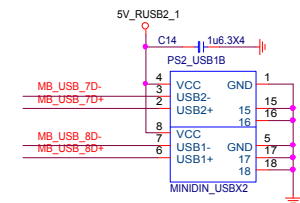
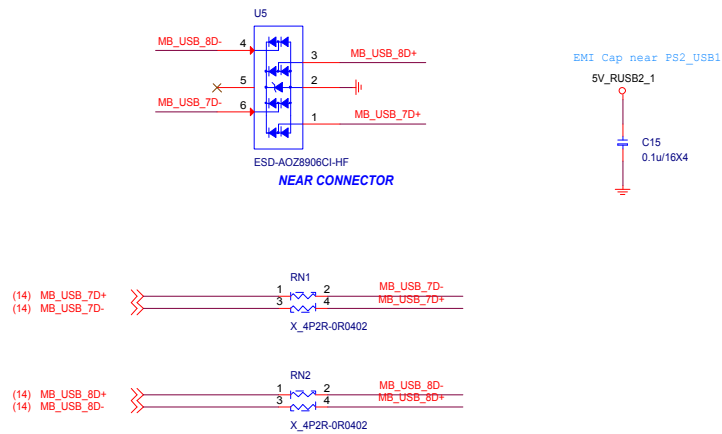
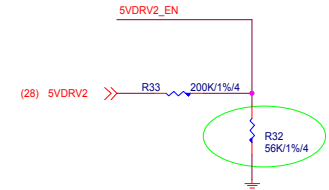
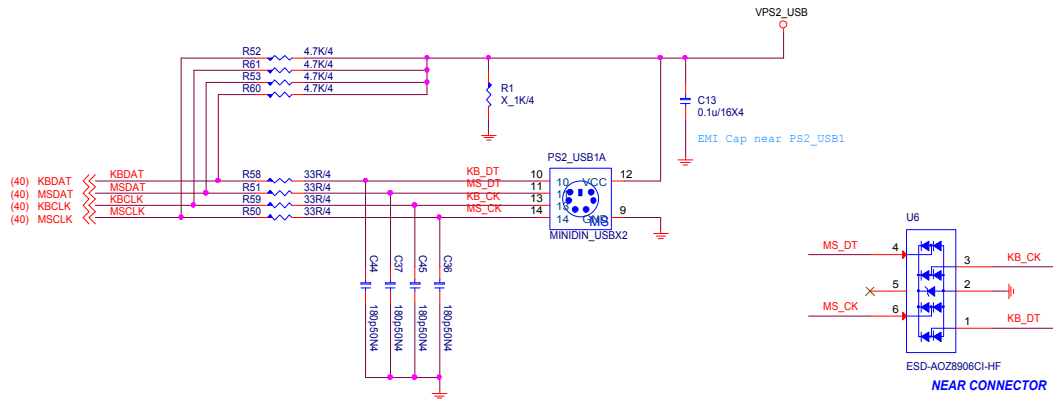
1.0A



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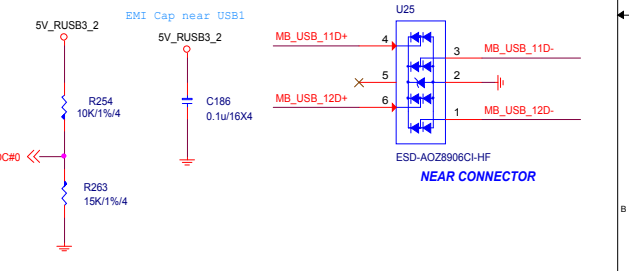
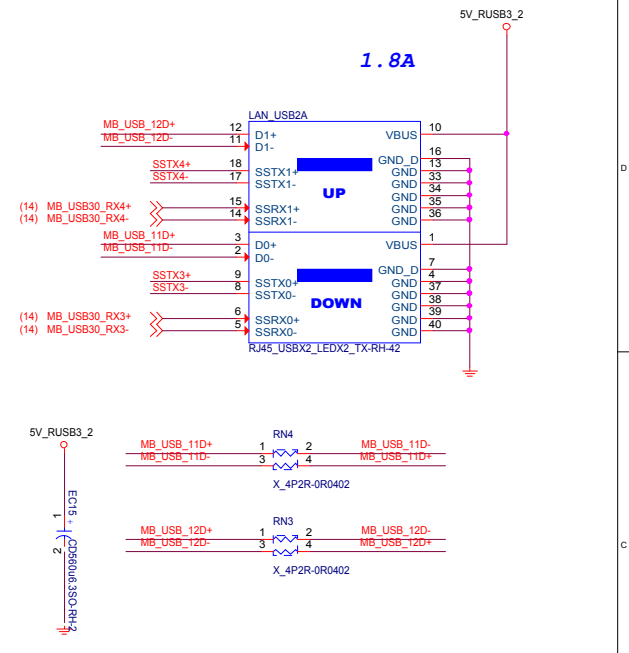
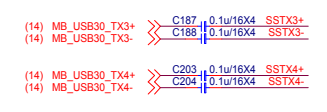
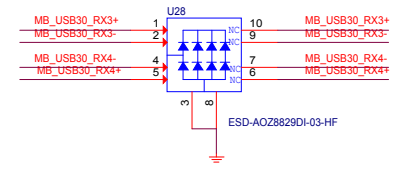
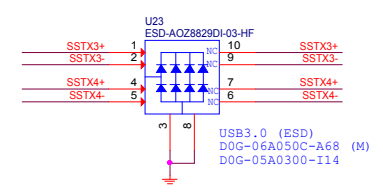
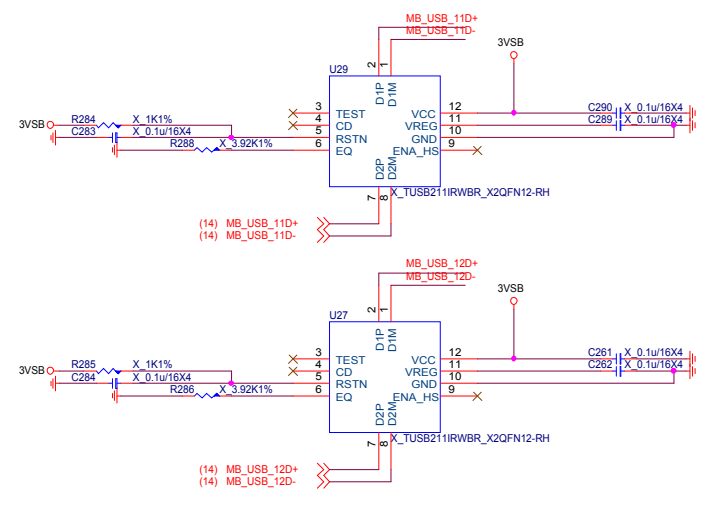
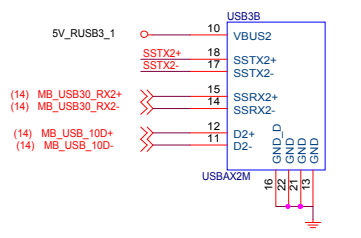
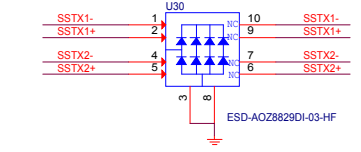
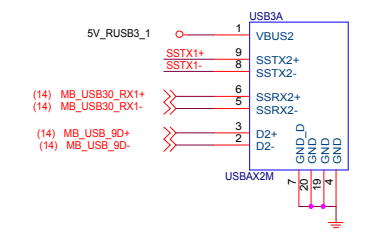
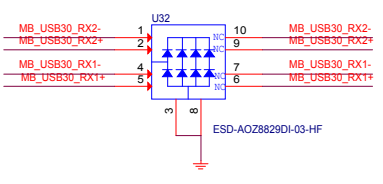
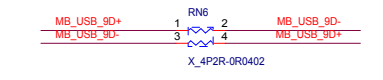
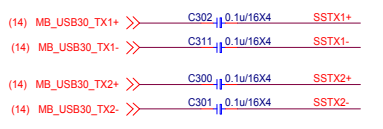
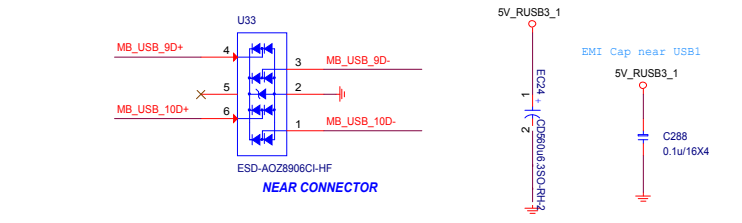


USB MODE

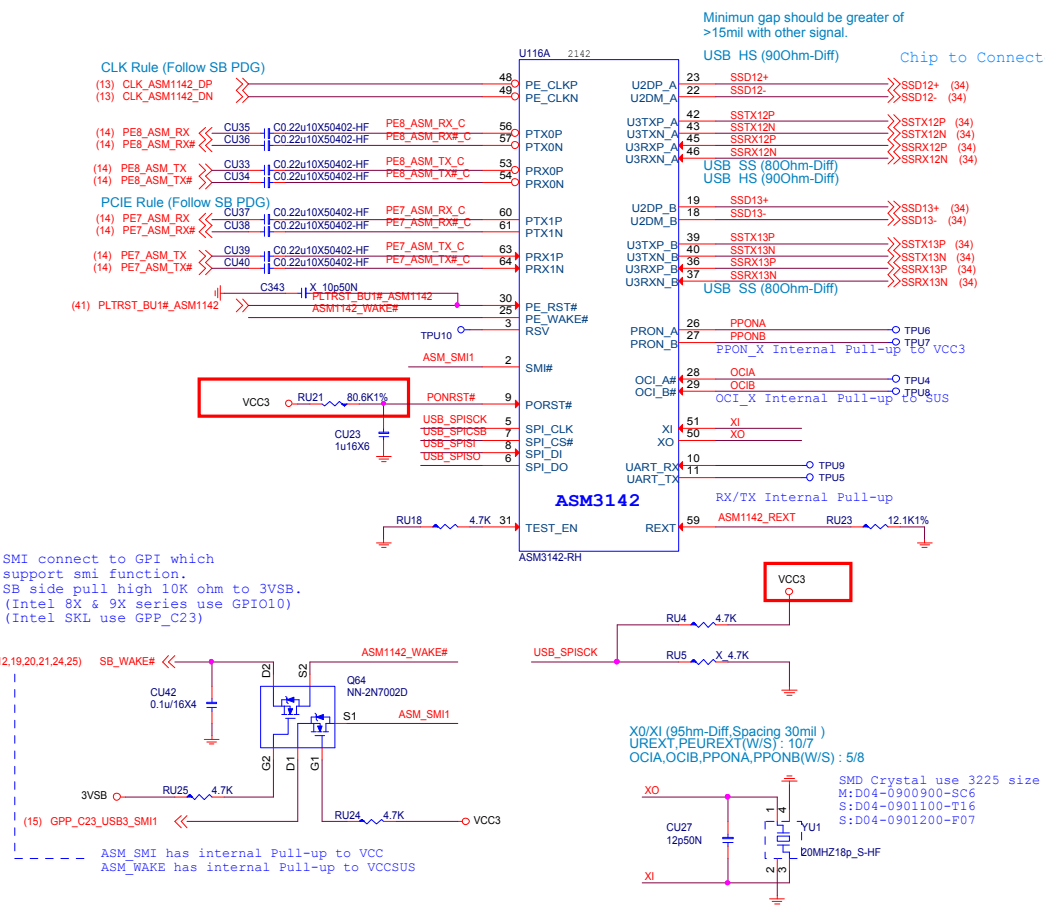
[illegible]

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Date: Tuesday, June 27, 2017	Sheet 31 of 69	



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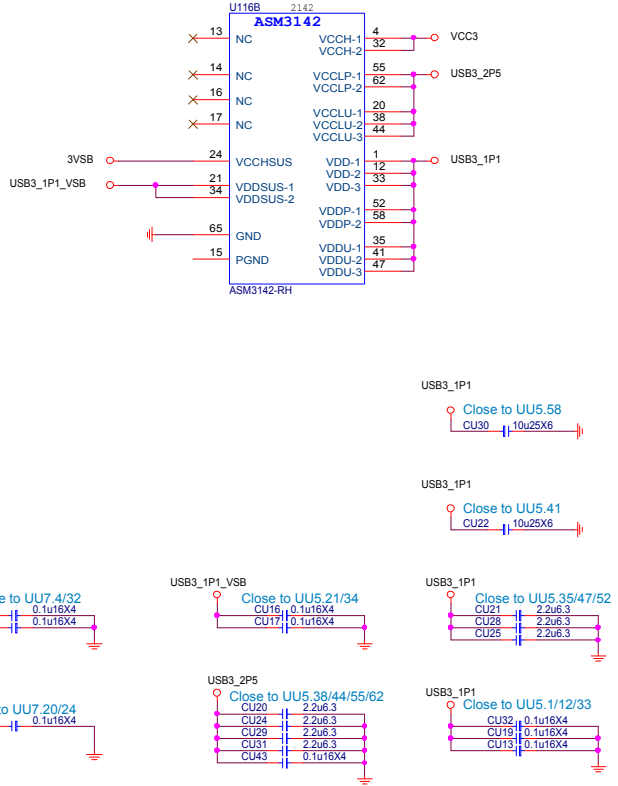


Layout Guide:

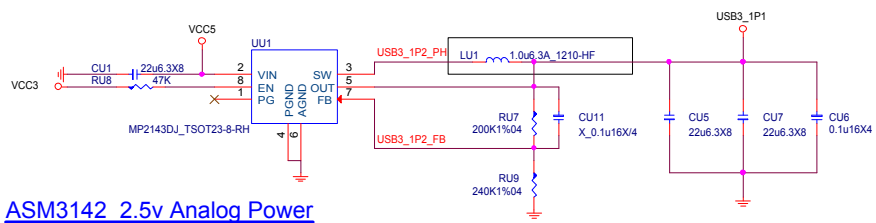
1.) USB3.1 to Connector Total Length < 1.5"

2.) VIA hole < 2

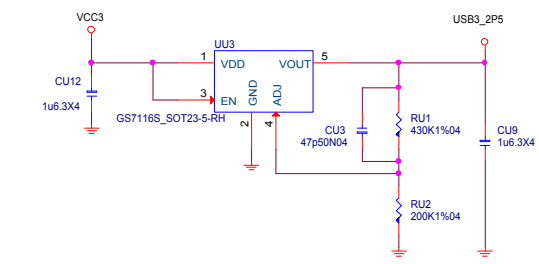
Power Consumption	3.3V	3.3VSUS	2.5V	1.1V	1.1VSUS	Unit
ASM3142	TbD	TbD	TbD	TbD	TbD	mA
ASM2142	4	9	220	470	10	mA



ASM3142 1.1v Core Power



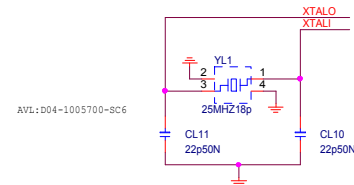
ASM3142 2.5v Analog Power



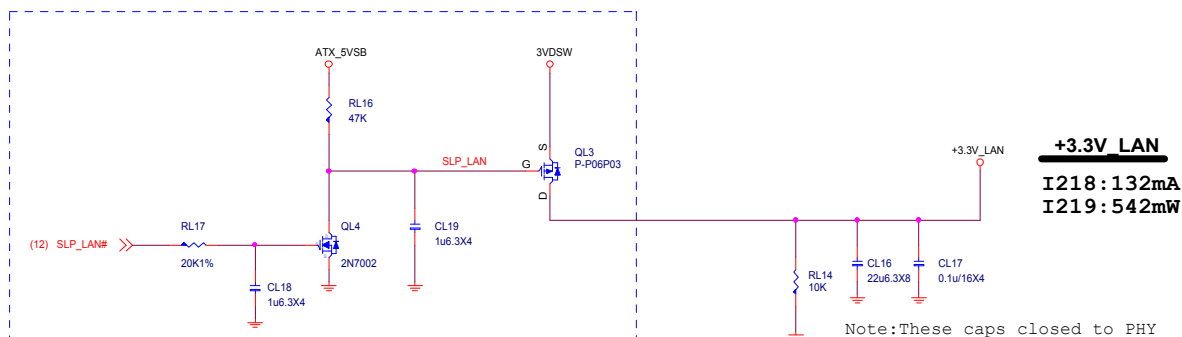
8111H:B06-08111CC-R09
8111G:B06-081116C-R09



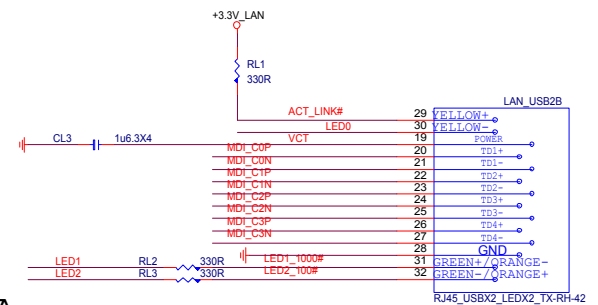
(13) LAN_CLKREQ#



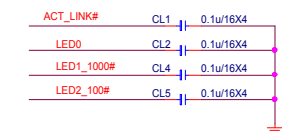
support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



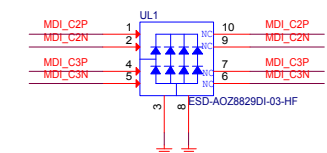
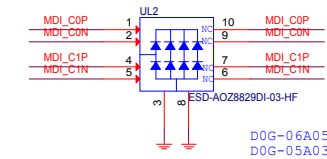
LAN Connector



For EMI



UL2&UL3 close to connector

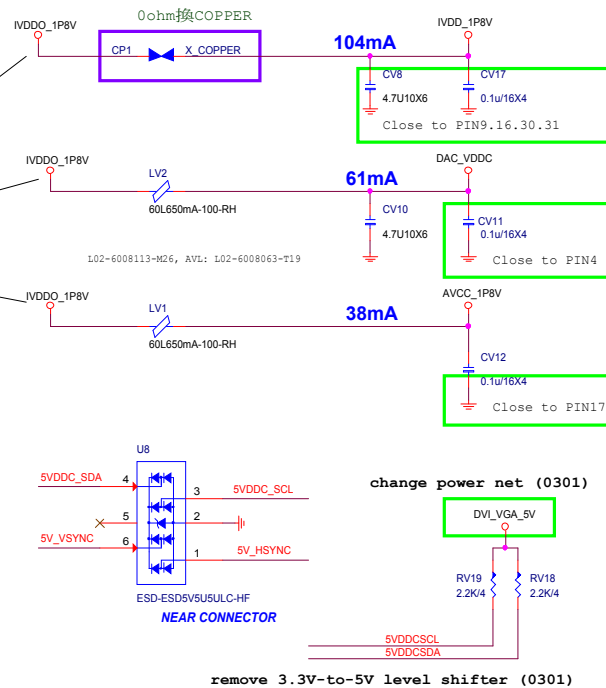
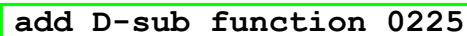


Do not pair MDI0 and MDI1 on the same TVSdevice
(avoid LAN POE connecting issue).
Otherpairing combination is ok.

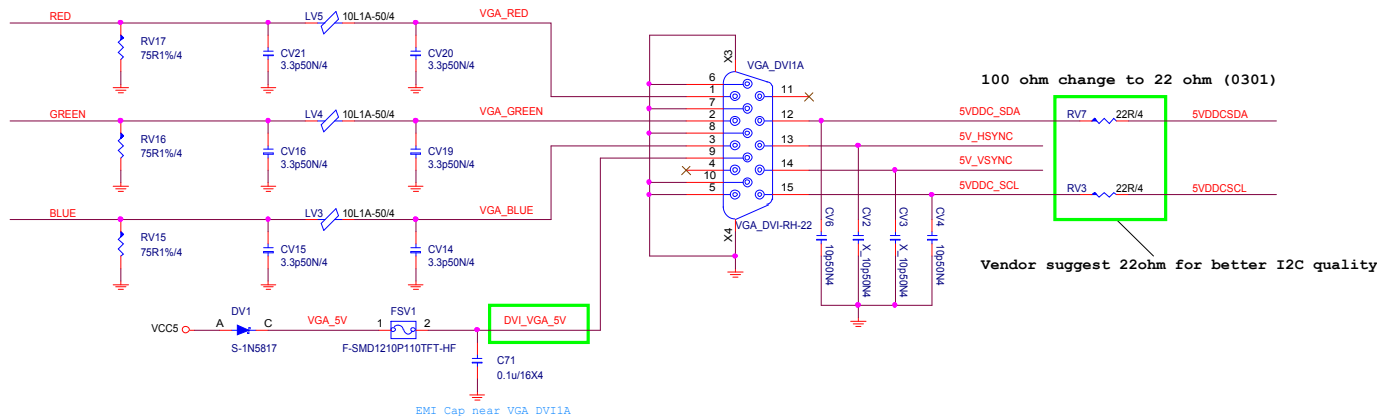
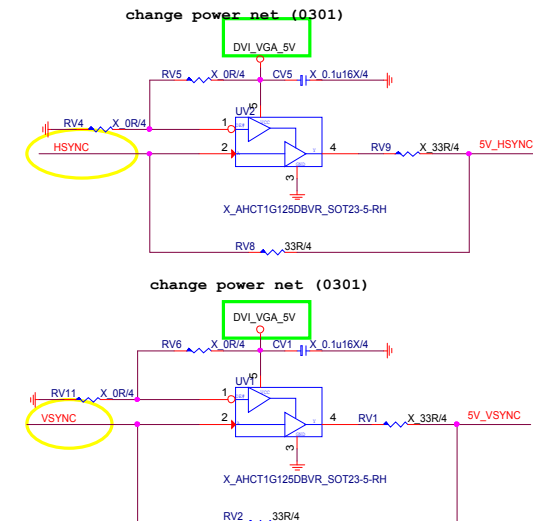
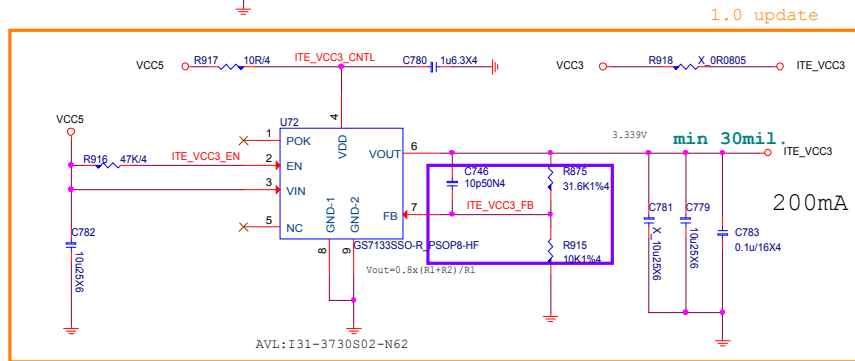


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Size Custom	Document Description Intel Lan- i219		Rev 1.0
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If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



System Status	GPIO	IT6516b's HPD
Legacy Mode (VBIOS) /DOS MOde	HIGH	Force HIGH
Windows /UEFI Mode (GOP)	LOW	Depend on VGA device's plug/unplug



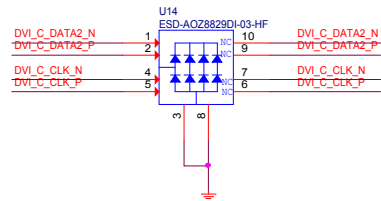
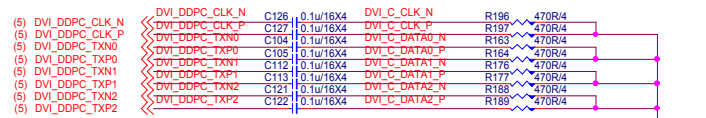
MICRO-STAR INT'L CO.,LTD

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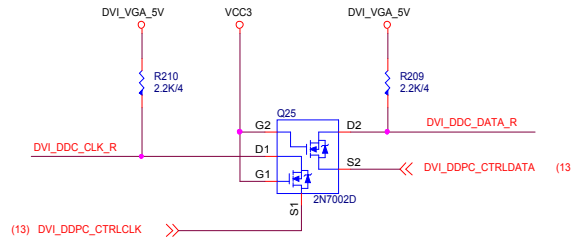
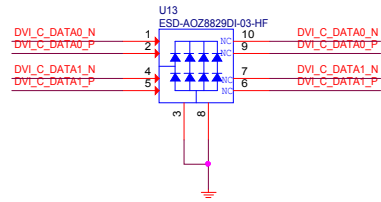
Size Custom	Document Description VGA - ITE6516	Re
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VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

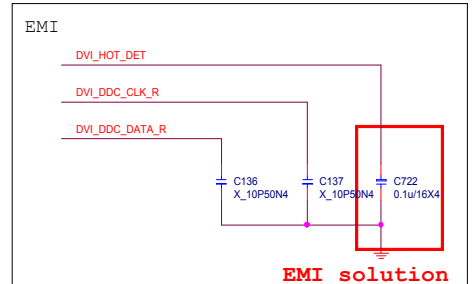
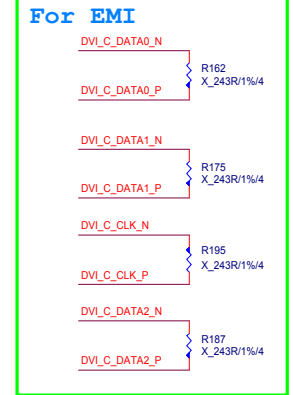
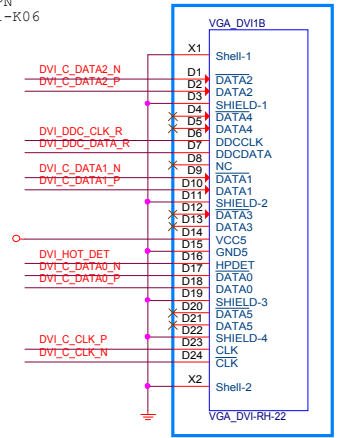
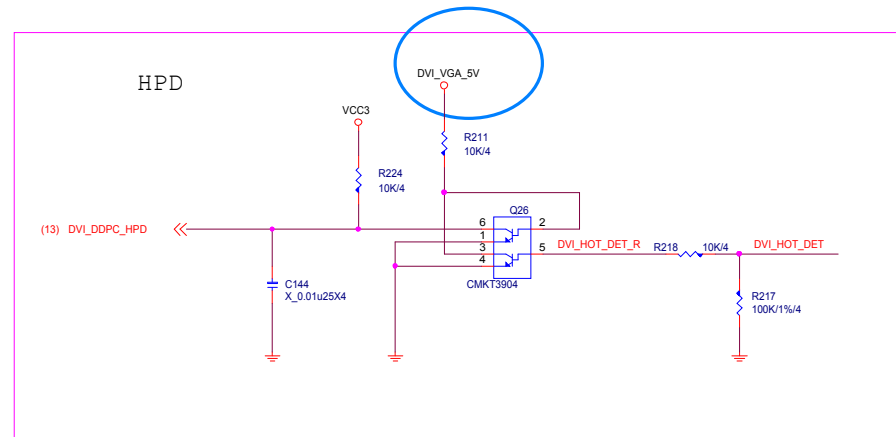
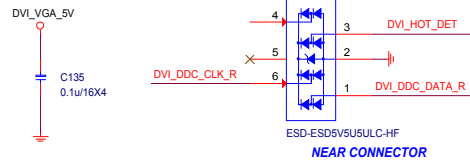
Check MSI PN
N58-39F0231-K06



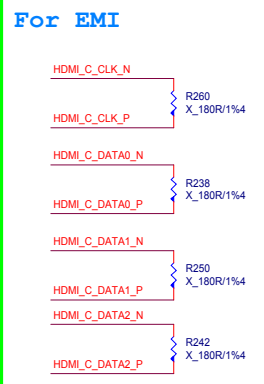
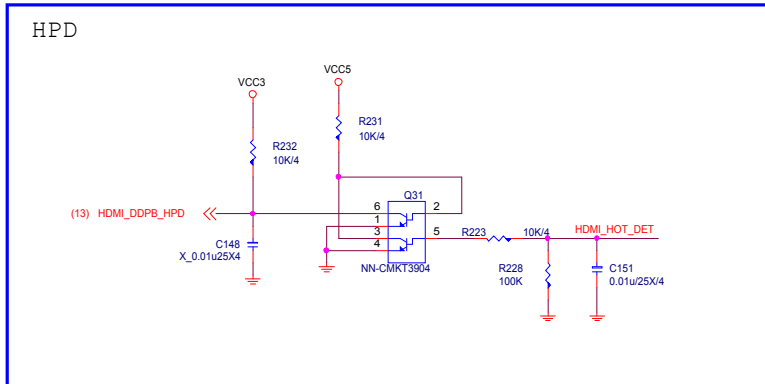
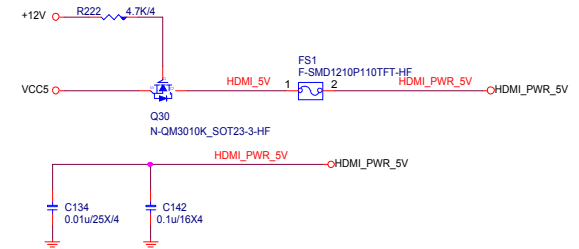
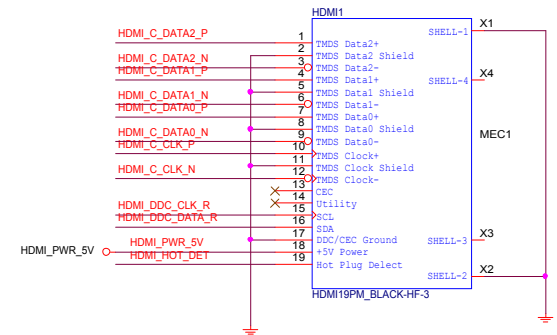
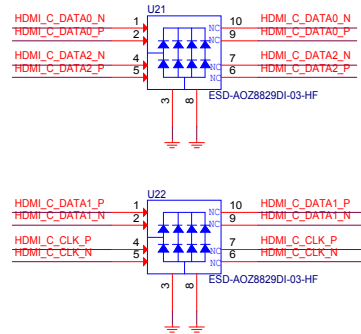
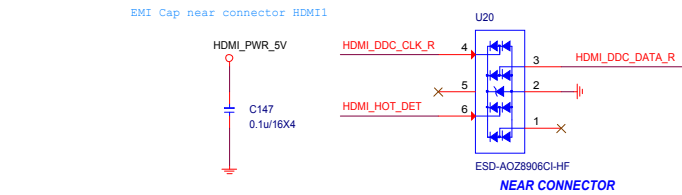
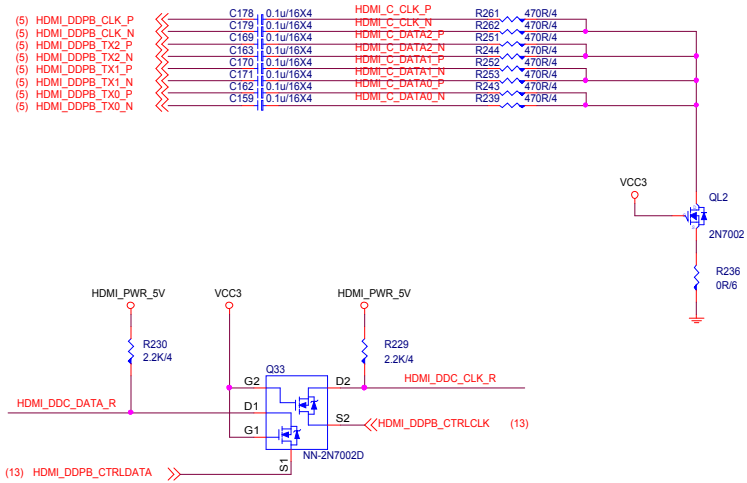
U27 AVL:D0G-05A050C-005
D0G-06A050C-A68




EMI Cap near connector DV11



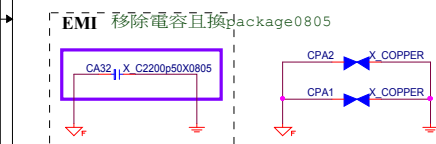
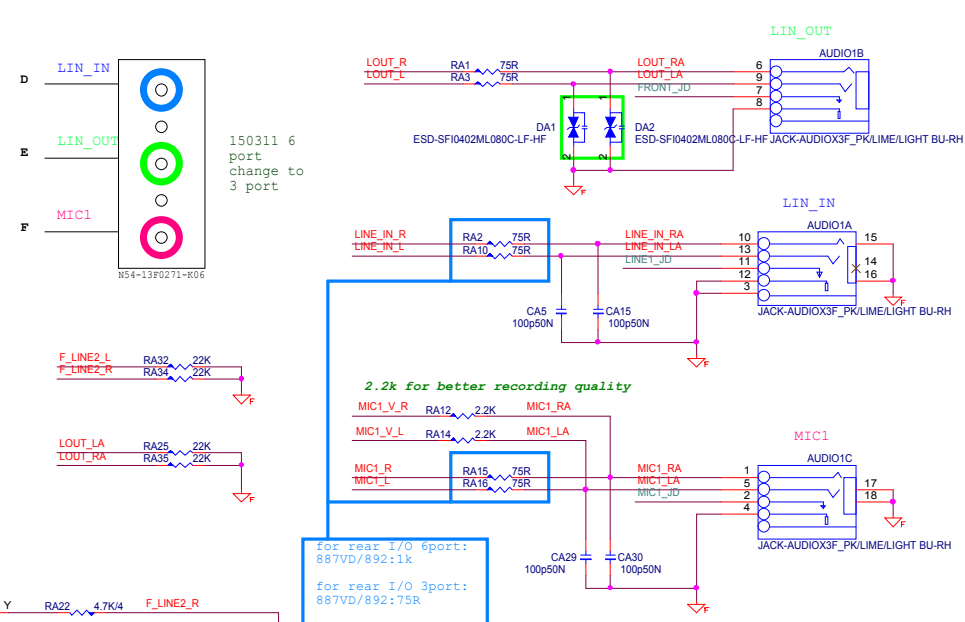
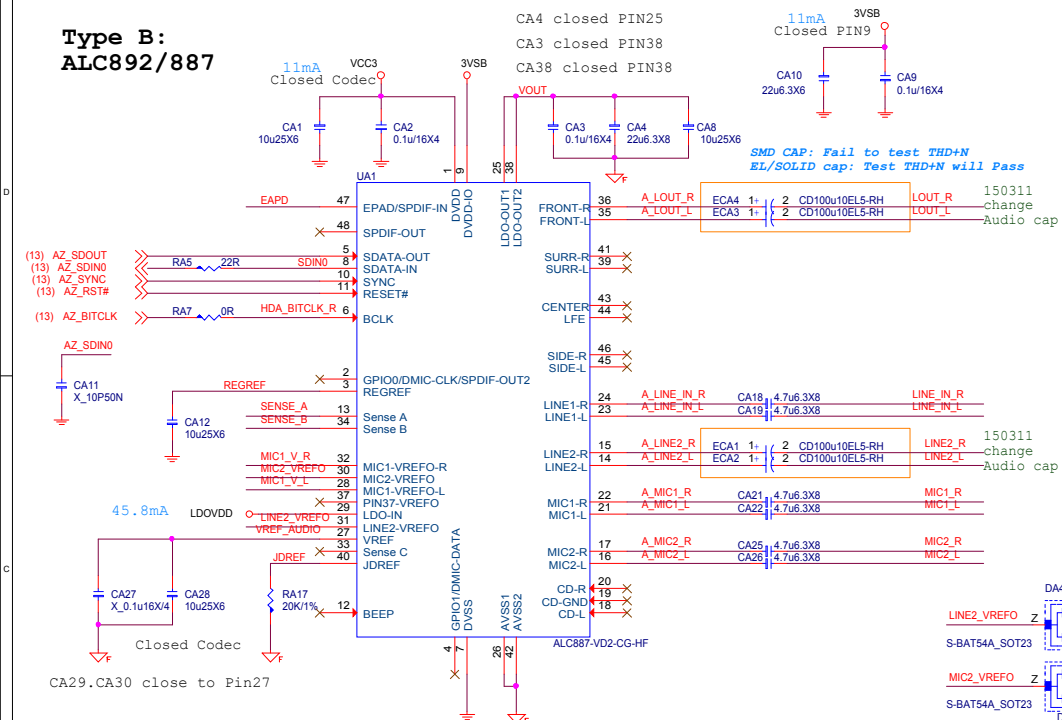
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



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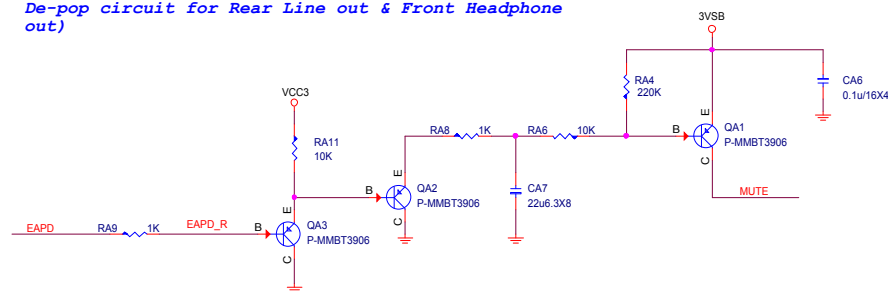
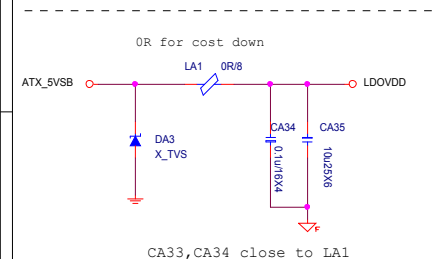
			
MICRO-STAR INT'L CO.,LTD			
MS-7B49			
Size	Document Description	Rev	
Custom	HDMI Connector	1.0	
Date: Tuesday, June 27, 2017	Sheet	38	of 69

Type B:
ALC892/887



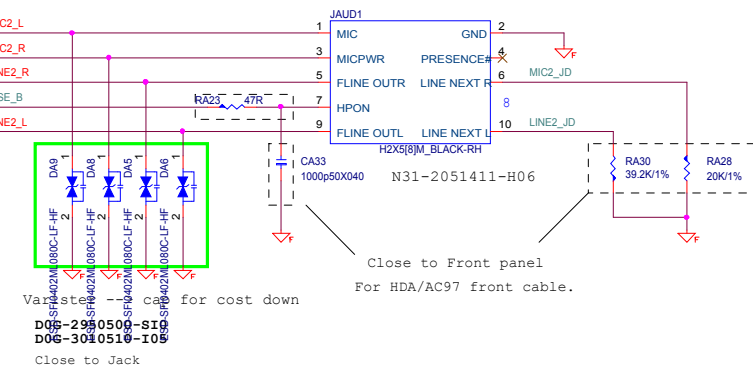
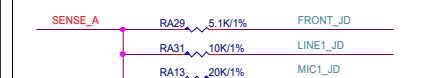
Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



Digital

Analog



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MS-7B49

Size	Custom
------	--------

	Document Description
	AUDIO A

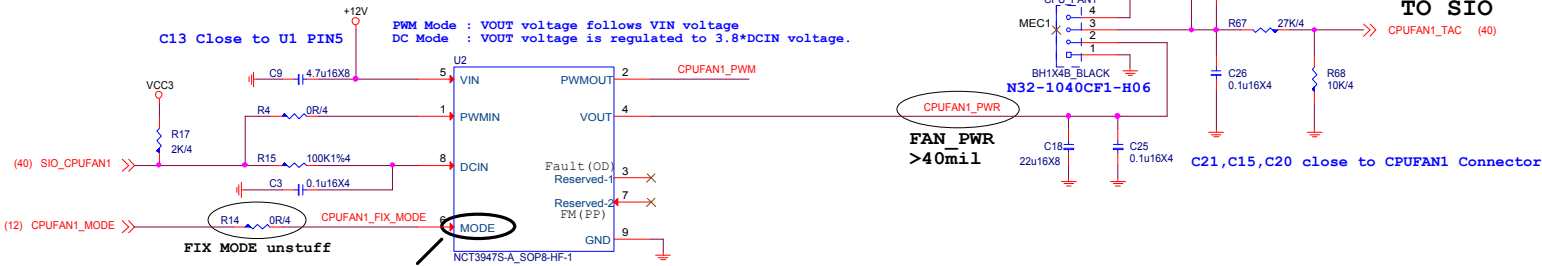
Rev	1.0
-----	-----

Date: Tuesday, June 27, 2017

Sheet 39 of 69

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

- 1.PWM/DC/OCF LED (現在是改成R/G/B3色LED)
- 2.GPIO可以由BIOS切換 PWM/DC MODE
- 3.OCF拉回GPIO給BIOS認
- 4.PWM OR DC FAN拉回GPIO給BIOS認
- 5.FAN轉速加快的時候由SOFTWARE 控制GPIO讓燈的變化

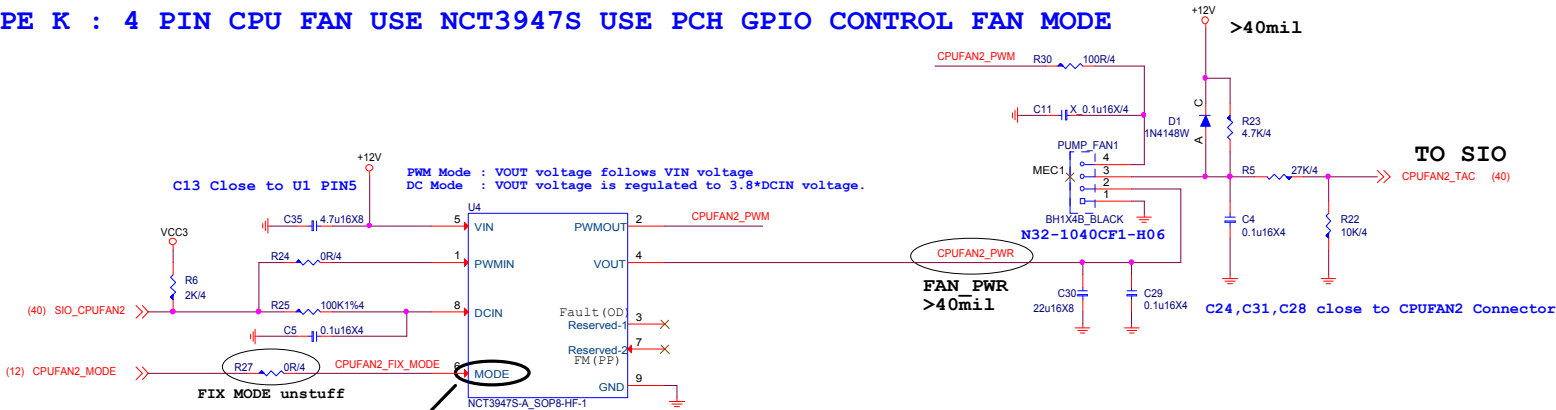


GPIO Control

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)

Default Internall pull up 1.65V

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



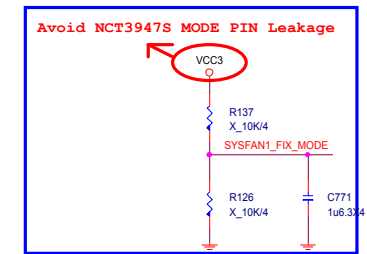
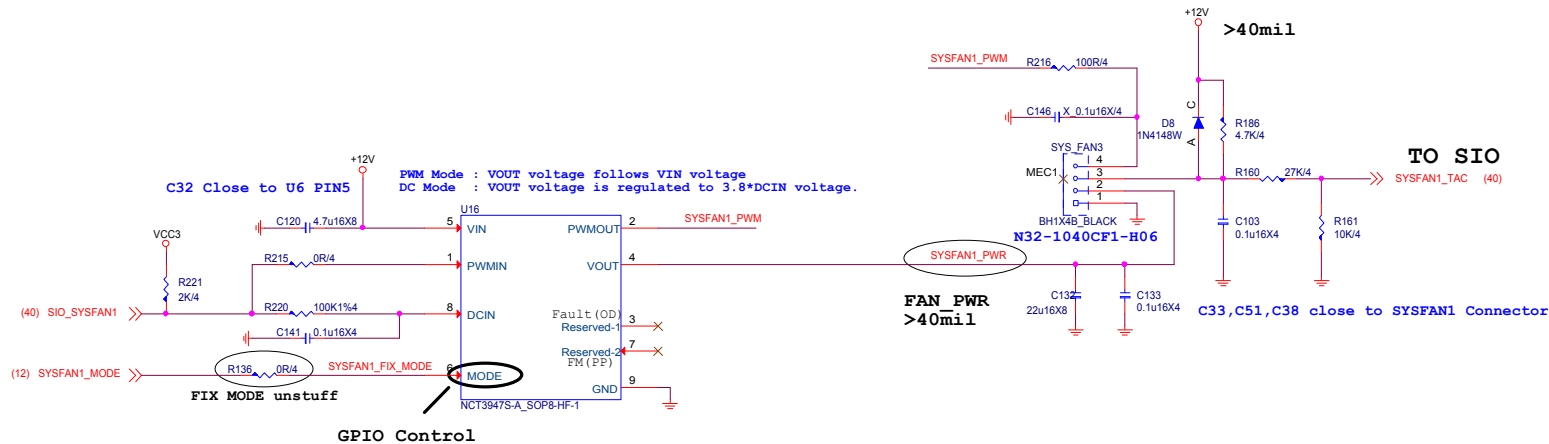
GPIO Control

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)

Default Internall pull up 1.65V

- 1.MODE : USE MODE PIN change FAN MODE(PWM or DC FAN)
- 2.FAULT : USE FAULT PIN Triger OVT/OCF Protection,LOW Atcive (Reserve NEW IC)
- 3.FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information(Reserve NEW IC)

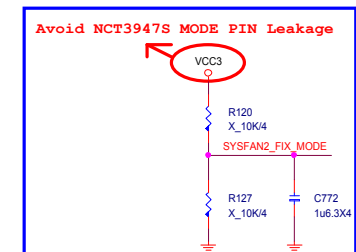
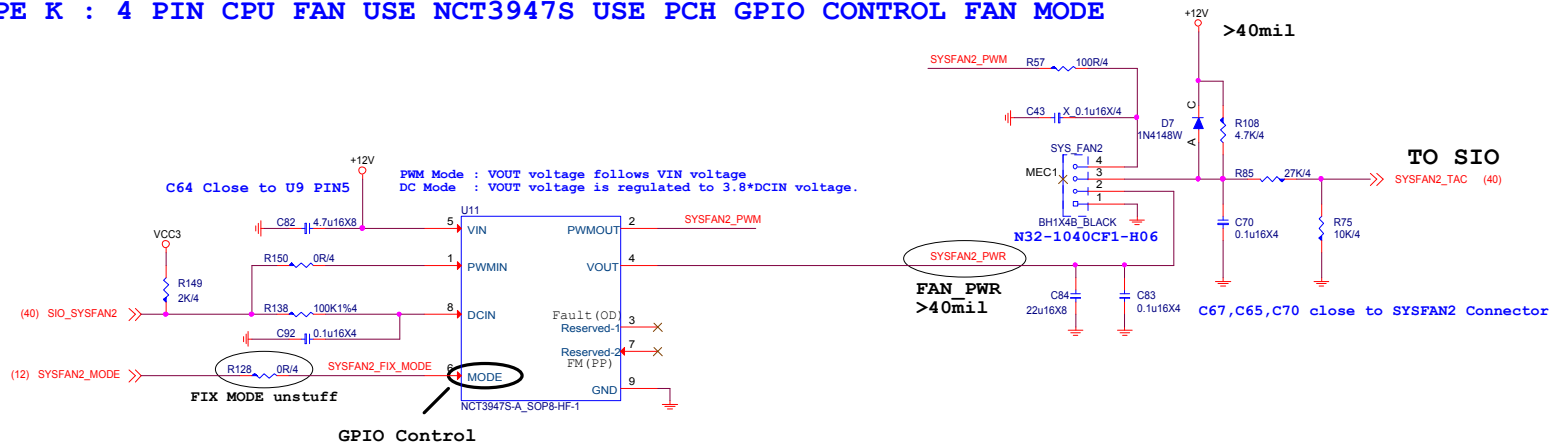
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default Internall pull up 1.65V

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

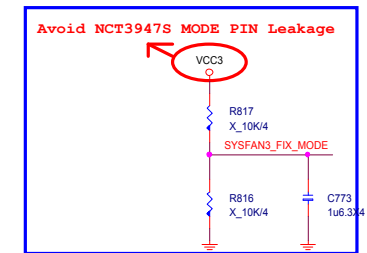


	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default Internall pull up 1.65V

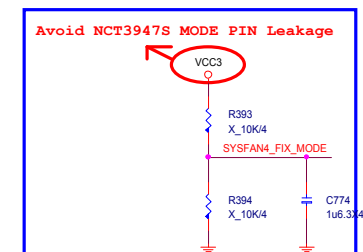
Vinafix.com

5	4	3	2	1
---	---	---	---	---



	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI (Floating)

internall pull up 1.65V

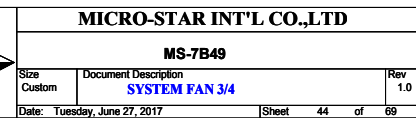


	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)

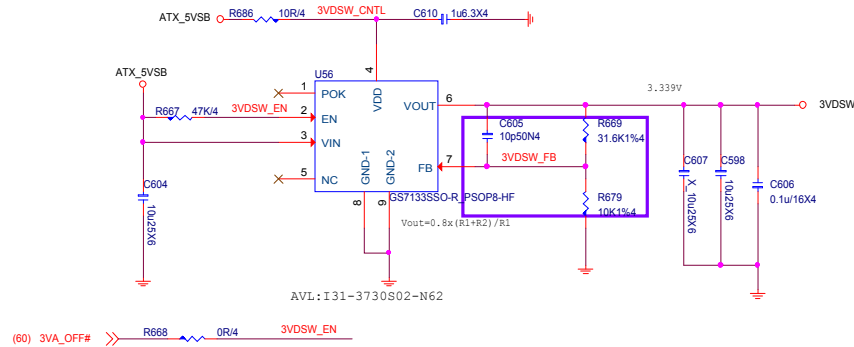
Default

Internall pull up 1.65V

A	MICRO-STAR INT'L CO. LTD.
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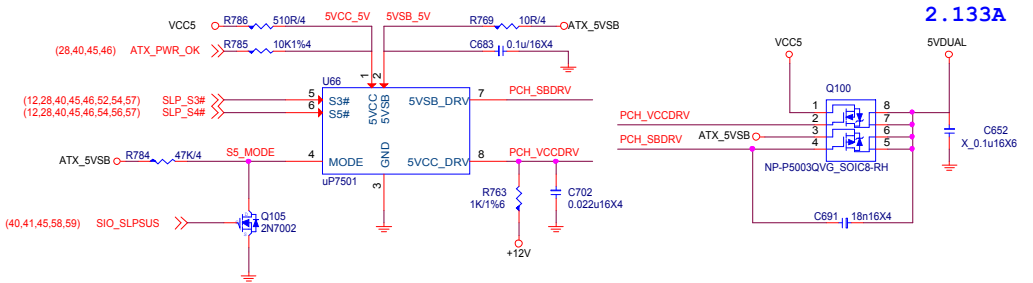


3VDSW

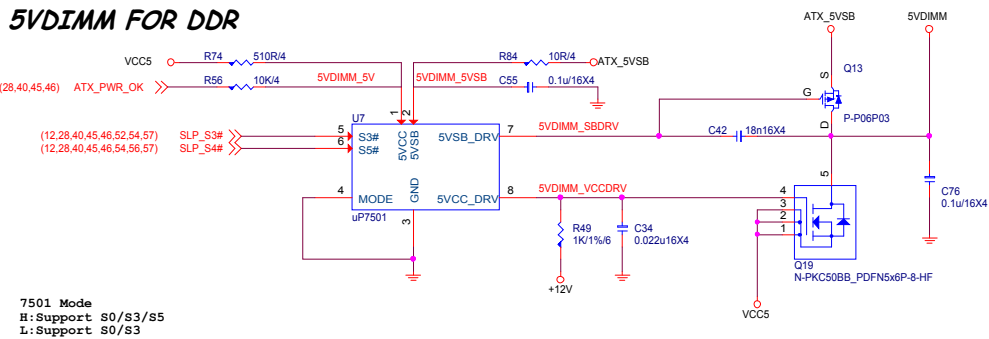


5VDUAL

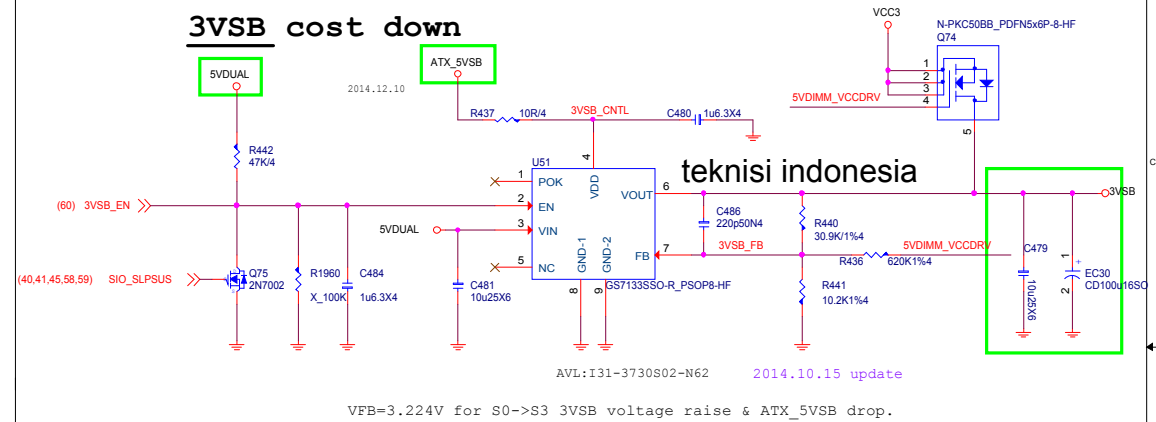
5VDUAL is power source of 1P0SB



5VDIMM FOR DDR



3VSB cost down



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[illegible]

The diagram shows the front panel circuitry. At the top, the **H1X4M_BLACK-RH-1** component is connected to a buzzer (BUZ) and a green LED (C155, 0.1u/16X4). The buzzer is also connected to a 1N4148W diode (D34) and a speaker (SPKR, 12, 18) via a 150R/8P4R resistor network (RN15). The speaker is connected to a 2N3904 transistor (Q11) and a 10K/4 resistor (R890). The **H2X510M_BLACK-RH** component is connected to a VCC5 supply via a 330R/6 resistor (R901) and a 0.1u/16X4 capacitor (C764). It also has connections for IDE_LED, RESET-, RESET+, and PWSW+ pins. The IDE_LED is connected to a 33R/4 resistor (R873) and a 0.1u/16X4 capacitor (C745). The RESET- pin is connected to a 33R/4 resistor (R873) and a 0.1u/16X4 capacitor (C756). The RESET+ pin is connected to a 100R/1%4 resistor (R900) and a 0.1u/16X4 capacitor (C755). The PWSW+ pin is connected to a 100R/1%4 resistor (R900) and a 0.1u/16X4 capacitor (C755). The PWSW- pin is connected to a 100R/1%4 resistor (R900) and a 0.1u/16X4 capacitor (C755). The PLED and SLED pins are connected to a 100R/1%4 resistor (R900) and a 0.1u/16X4 capacitor (C755). The PSIN#_R pin is connected to a 100R/1%4 resistor (R900) and a 0.1u/16X4 capacitor (C755). The PWRBTIN pin is connected to a 100R/1%4 resistor (R900) and a 0.1u/16X4 capacitor (C755).

[illegible]

The schematic diagram illustrates the electrical connections for the ATX Power/F_Panel, specifically focusing on the TPM module and the ATX Power/F_Panel components.

TPM Module Connections:

- TPM_CLK:** Connected to pin 1 of JTPM1.
- PLTRST_BU3#_TPM:** Connected to pin 3 of JTPM1.
- LPC_AD0:** Connected to pin 5 of JTPM1.
- LPC_AD1:** Connected to pin 7 of JTPM1.
- LPC_AD2:** Connected to pin 9 of JTPM1.
- LPC_AD3:** Connected to pin 11 of JTPM1.
- LPC_FRAME#:** Connected to pin 13 of JTPM1.

ATX Power/F_Panel Connections:

- 3VSB:** Connected to pin 2 of JTPM1.
- VCC3:** Connected to pin 4 of JTPM1.
- SERIRQ_R:** Connected to pin 6 of JTPM1.
- VCC5:** Connected to pin 8 of JTPM1.

Other Components and Connections:

- R801:** A 0R/4 resistor connected between SERIRQ_R and SERIRQ (12,40).
- C693:** A 0.1u/16X4 capacitor connected between 3VSB and ground.
- C340:** A 0.1u/16X4 capacitor connected between VCC3 and ground.
- C287:** A 0.1u/16X4 capacitor connected between VCC5 and ground.
- C694:** A capacitor connected between X_C10p50N4 and PLTRST_BU3#_TPM.
- H2X7[10]M-2PITCH:** A connector pin header.

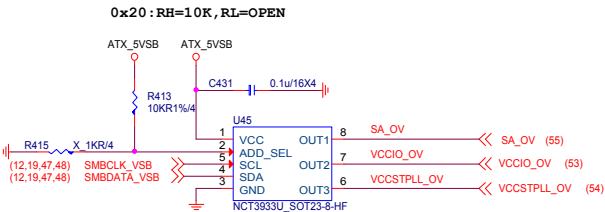
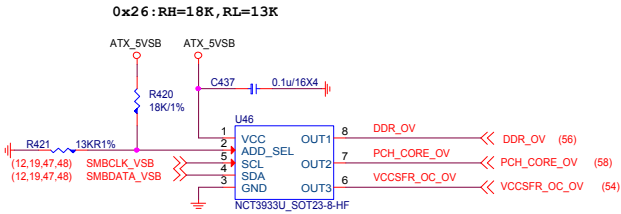
Legend:

- EMI:** Electro-Magnetic Interference.
- 3VSB:** Standby Voltage.
- VCC3:** Core Voltage.
- VCC5:** I/O Voltage.

Over Voltage Control IC

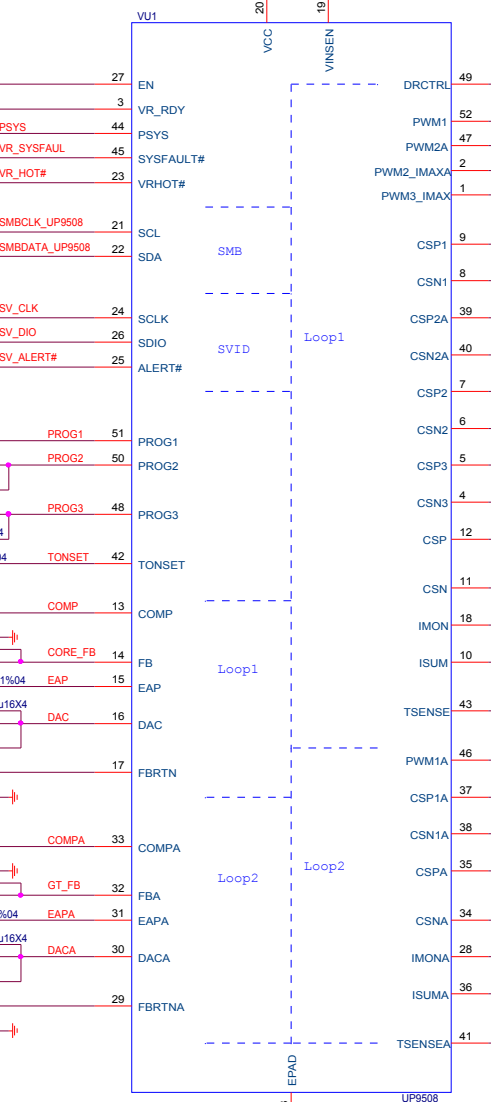
UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

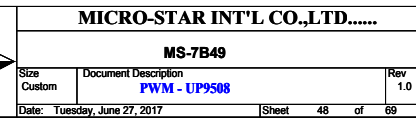
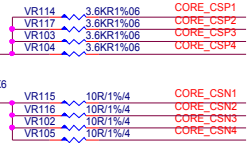
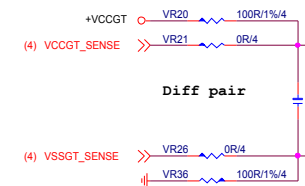


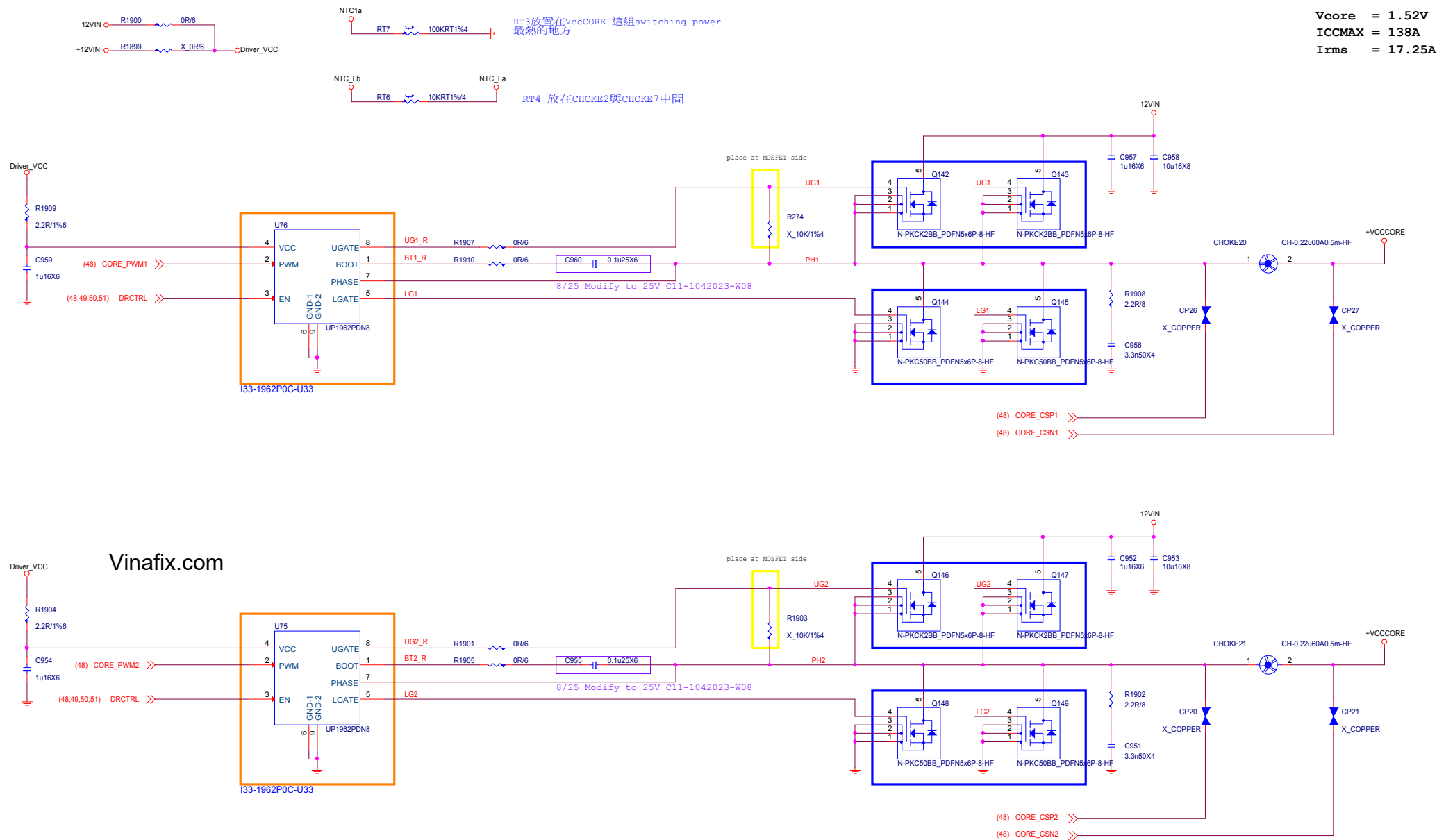
Vinafix.com

VGT: ICC Max 45A
LL: 3.1 mohm
OCP: 75A



R1889 1K/1%/4 DRCTRL (49,50,51)

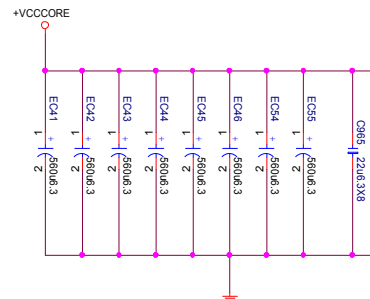
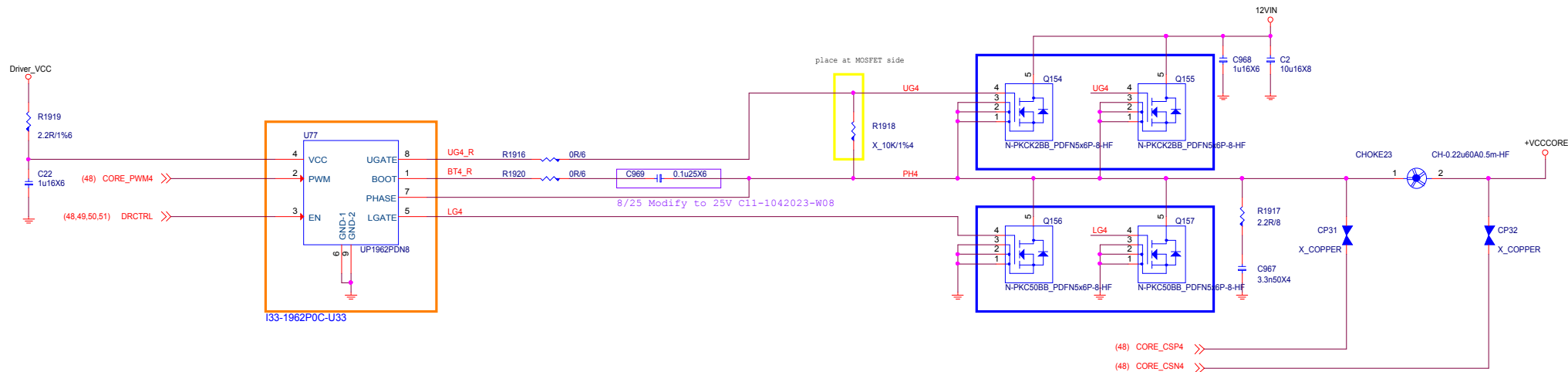
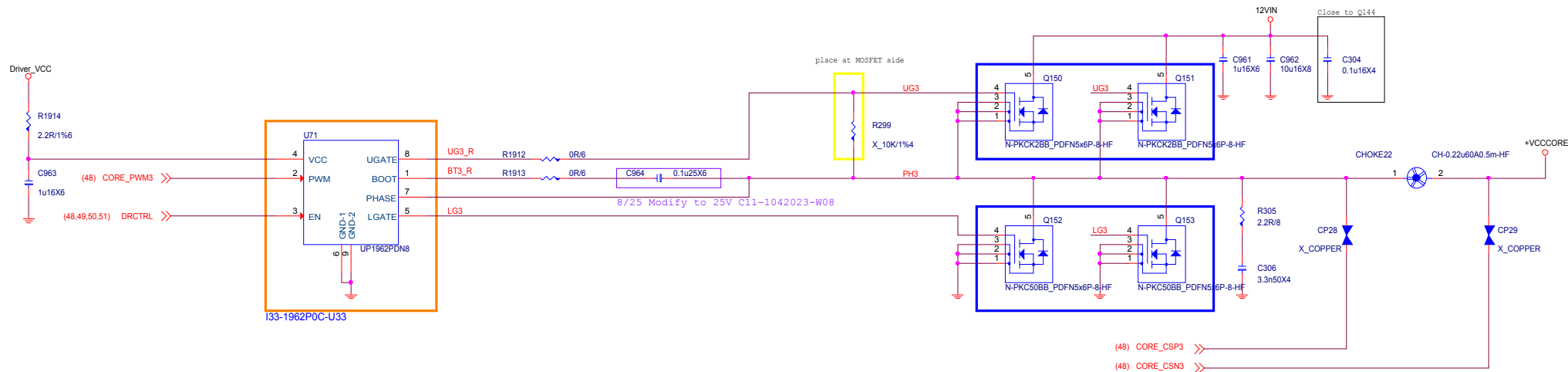




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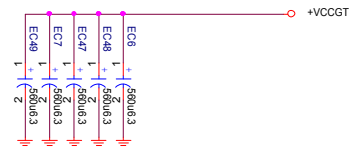
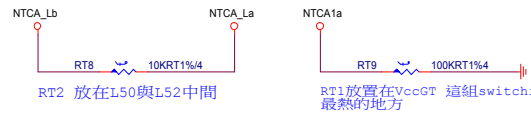
Size	Document Description	Rev
Custom	VCORE - PHASE 1-2	1.0
Date: Tuesday, June 27, 2017	Sheet 49 of 69	



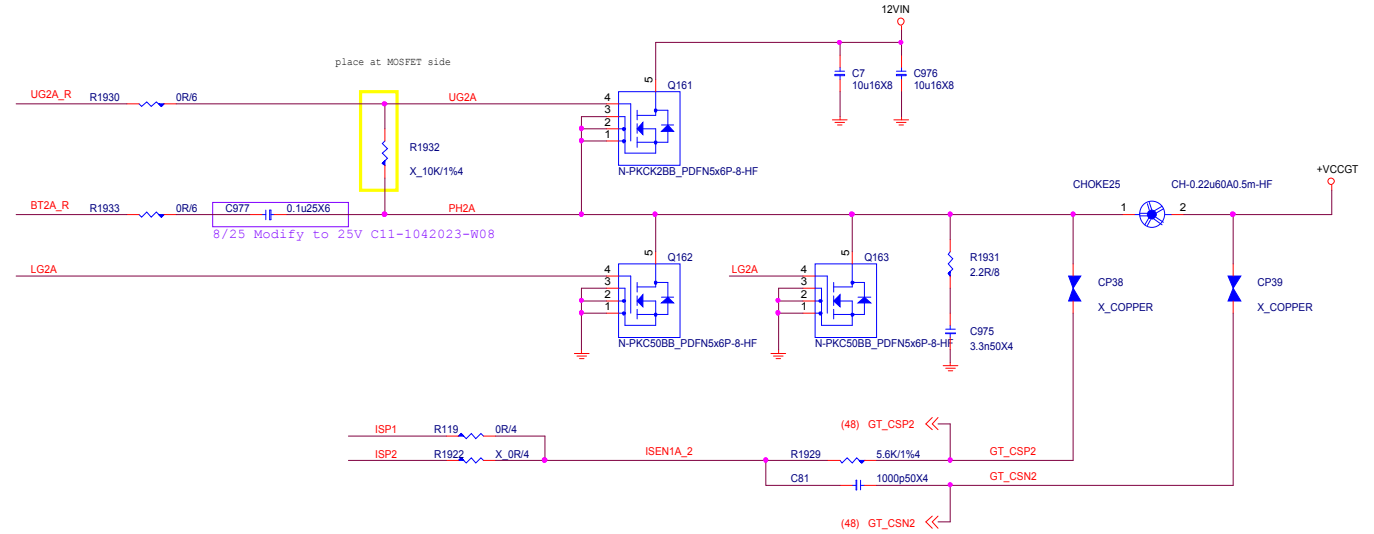
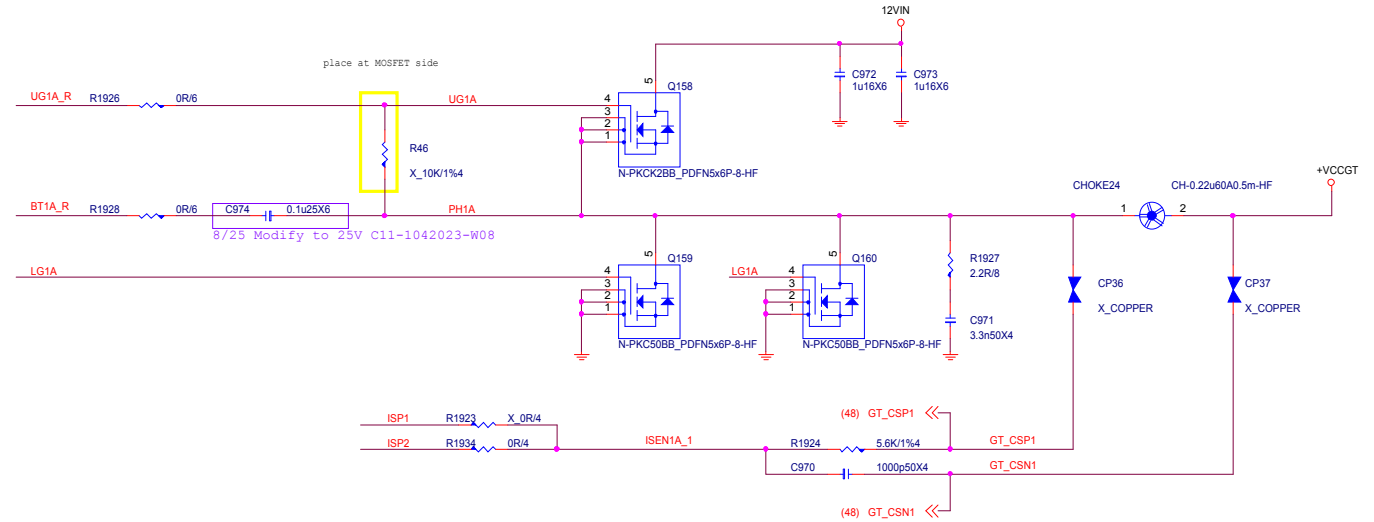
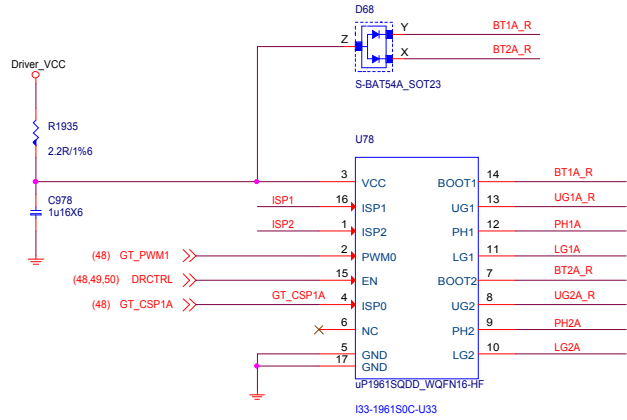
MICRO-STAR INT'L CO.,LTD

MS-7B49

Size	Document Description	Rev
Custom	VCORE - PHASE 2-4	1.0
Date: Tuesday, June 27, 2017	Sheet 50 of 69	



Vcore = 1.52V
ICCMAX = 45A
Irms = 9.79A

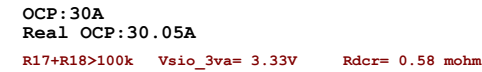
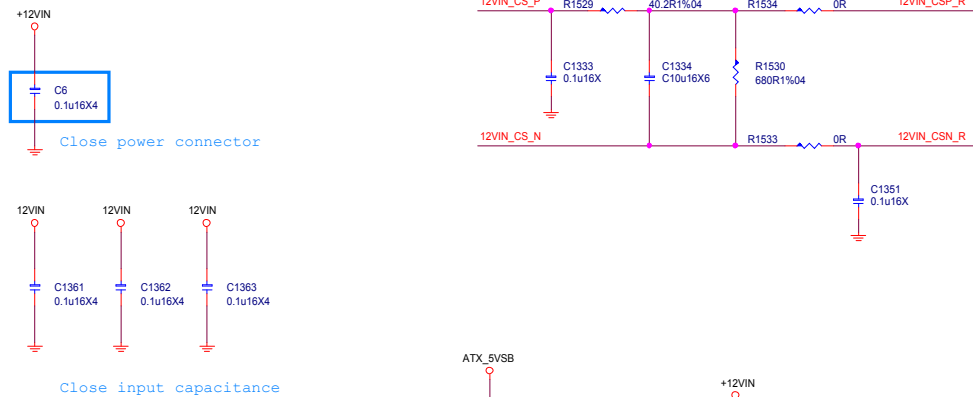


MICRO-STAR INT'L CO.,LTD

MS-7B49

Size	Document Description	Rev
Custom	VGT - PHASE 1-2	1.0
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```
Iripple = 27.04A
VCORE   = 17.25A
VGT      = 9.79A
```



```
I3933_imon*[R17*R18/(R17+R18)]= Istep* RdcR*100
I3933_imon= 10uA/step
Istep=4.785A
```



MS-7B49

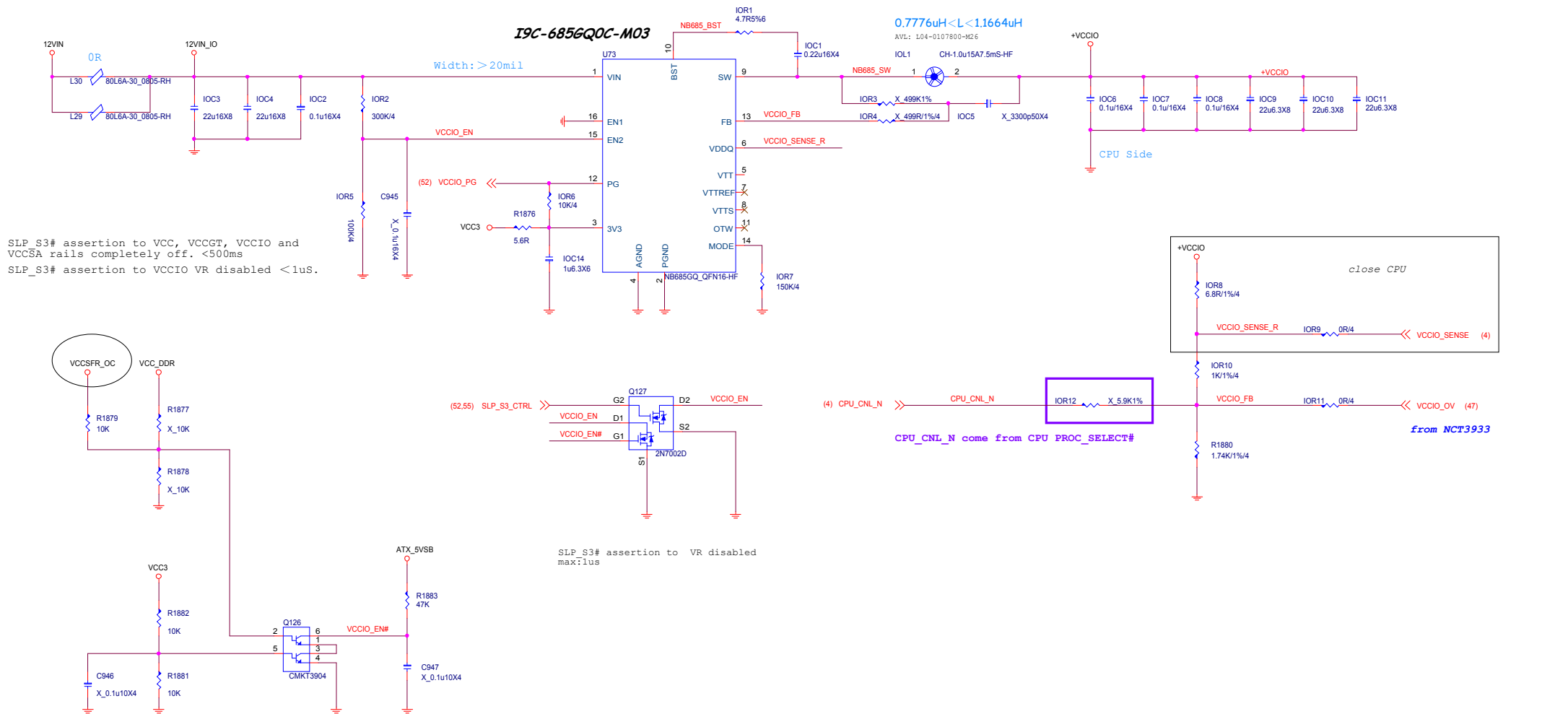
Size Custom	Document Description UP6273	Rev 1.0
Date: Tuesday, June 27, 2017		Sheet 52 of 69

VCCIO

0.95V ; 6.4A

IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

support OV=>NB685



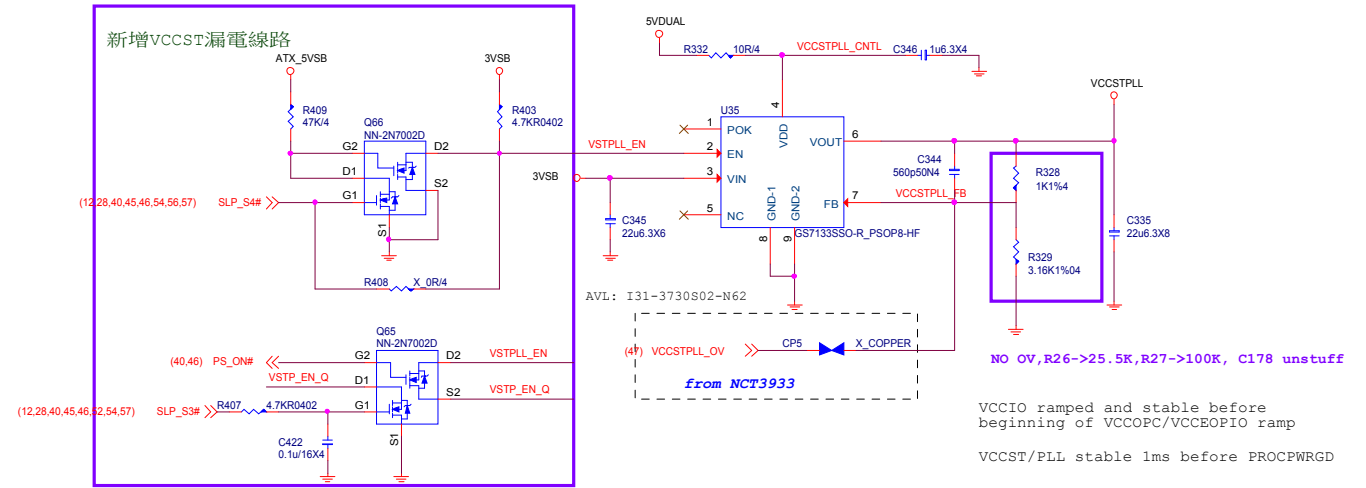
SLP_S3# assertion to VR disabled
max:1us

VCCSTPLL

1.0V; 250mA

For Cost down VCCST&VCCPLL merge

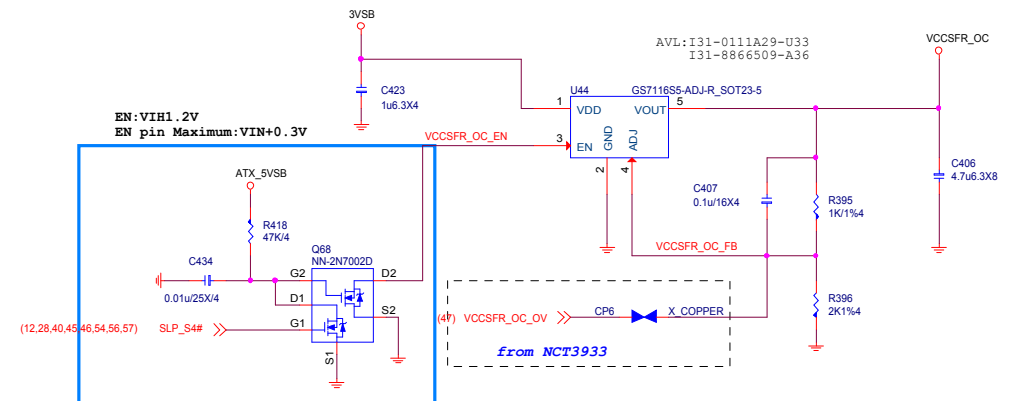
for Gaming3/5, Classic, ECO and H110



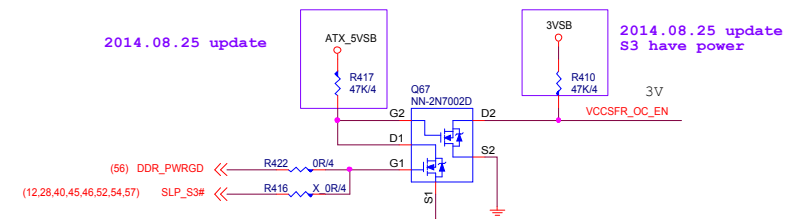
VCCPLL_OC

1.2V; 130mA

2014.08.21 update



2014.08.25 update



MICRO-STAR INT'L CO.,LTD			
MS-7B49			
Size	Document Description	Rev	
Custom	VCCST/PLL - GS7133/7116	1.0	
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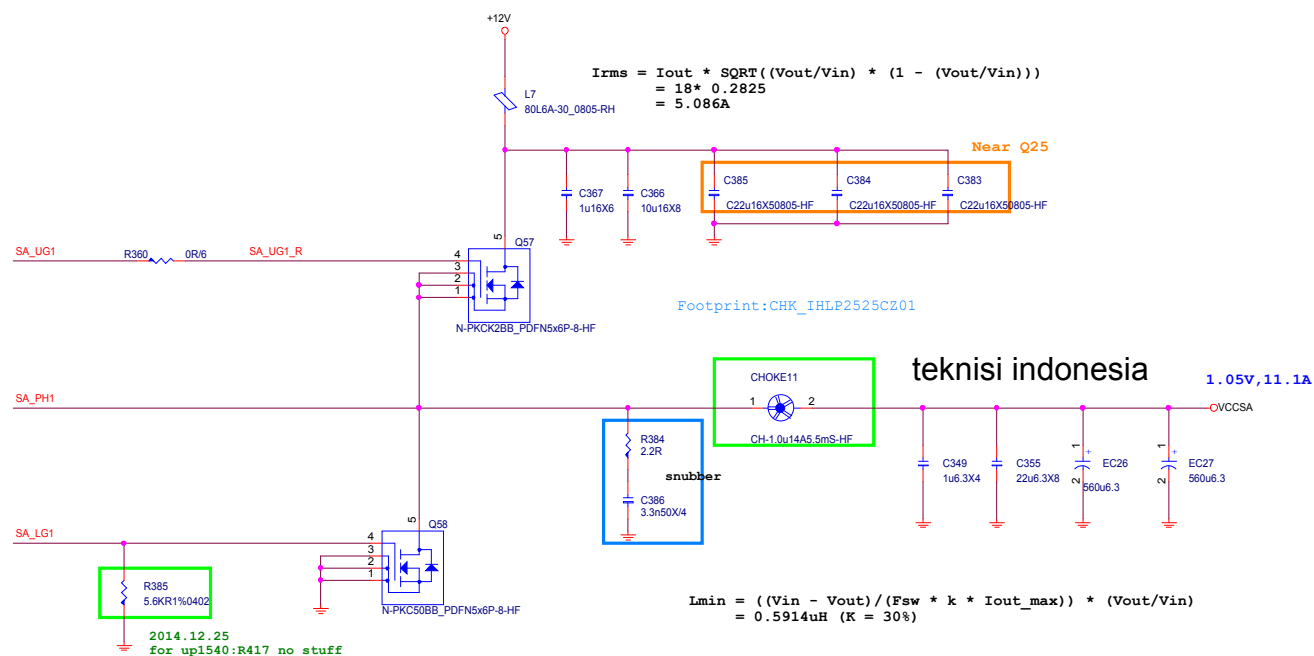
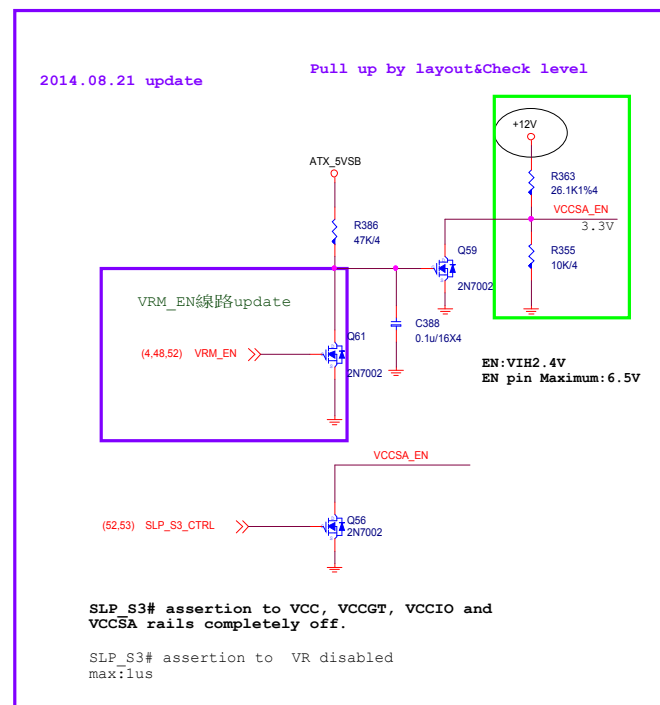
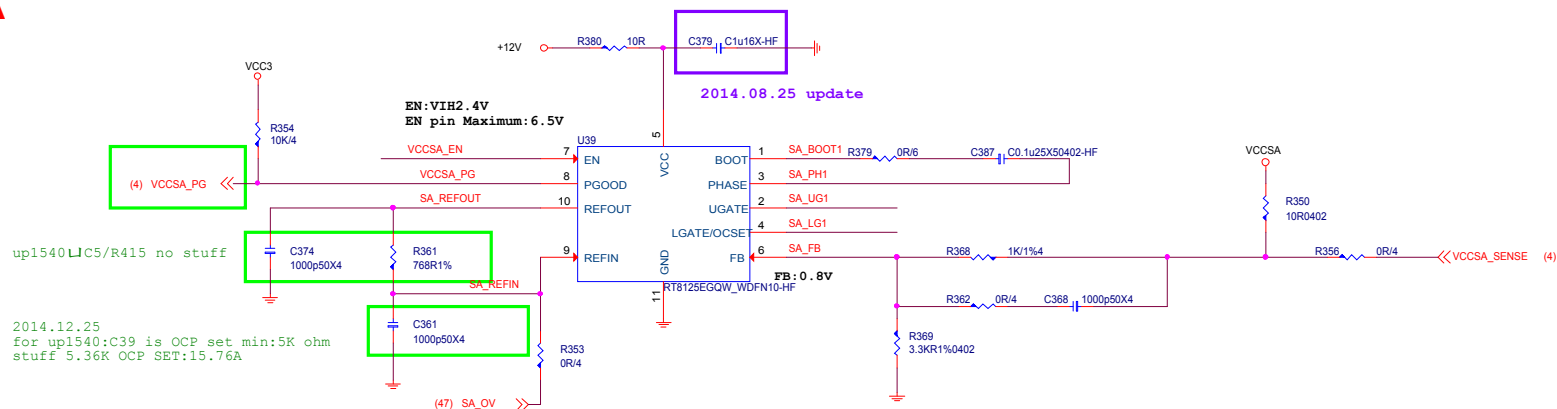
$$\begin{aligned} R_{ocpset} &= 5.6K \\ OCP &= R_{ocpset} * R_{dson}(\text{Low side}) / 10uA \\ &= 5.6K * 3.3mohm / 10uA \\ &= 18.48A \end{aligned}$$

```
Rocs:5.76K,OCP:
D03-4C05N03-O05 : 16.94A
D03-632BA0C-N03 : 17.45A
use UBIQ MOS need Check
```

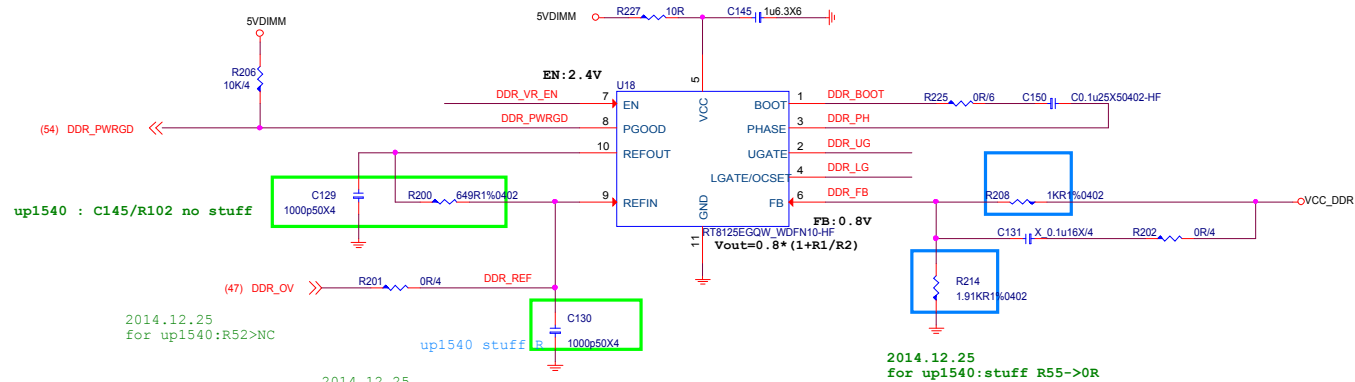
Rdson (low) 10V

D03-4C05N03-O05	:	3.4mohm
D03-632BA0C-N03	:	3.3mohm
D03-3056M00-U47	:	4.2mohm

Vsa = 1.05V
ICCMAX = 11.1A
Irms = 3.14A



3.3A FOR CPU
9.5A FOR 4DIMM
1.2A FOR DDR VTT

$$\begin{aligned} \text{Rocpset} &= 4.32\text{K} \\ \text{OCP} &= \text{Rocpset} * \text{Rdson}(\text{Low side}) / 10\mu\text{A} \\ &= 4.32\text{K} * 4.6\text{mohm} / 10\mu\text{A} \\ &= 19.87\text{A} \end{aligned}$$


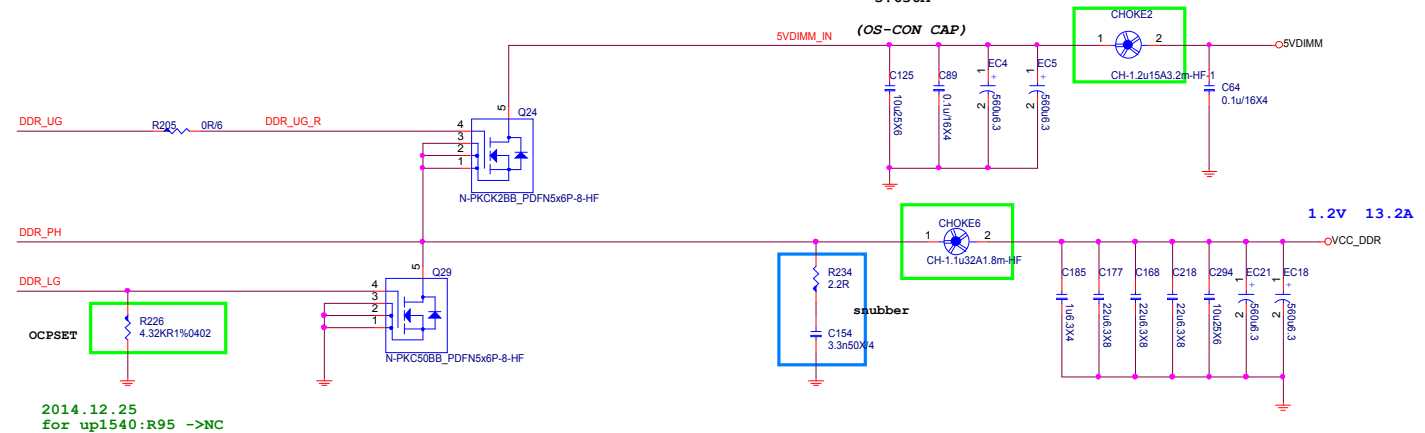
```
Rdson (low) 4.5V
D03-4C05N03-O05 : 5 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm
```

2014.12.25
for up1540:R52>NC

up1540 stuff R 1000p50X4

5
0:C125 is OCP set min:5K ohm
E 5.1K OCP SET:22.173A

```
Irms = Iout * SQRT{(Vout/Vin) * [1 - (Vout/Vin)]}
      = 13.2* 0.427
      = 5.636A
```



```
2014.12.25
for up1540:R95 ->NC
```

Datasheet公式計算

$$I_{min} = ((V_{in} - 1.2V) / (F_{sw} * k * I_{out_max})) * (V_{out} / V_{in})$$

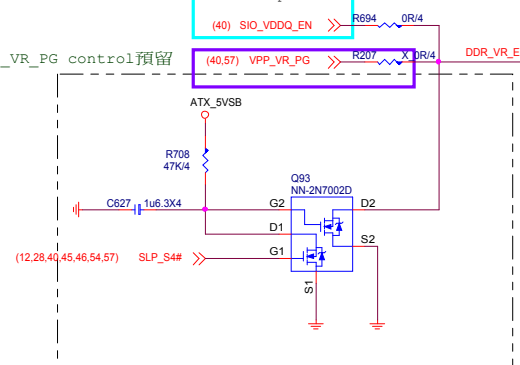
$$= 0.7677\mu H \quad (K = 30\%)$$

若帶入CAP ESR計算, $0.2432\mu\text{H} < L < 1.2897\mu\text{H}$

2014.12.17 update

From SIO pin 87

VPP_VR_PG control預留



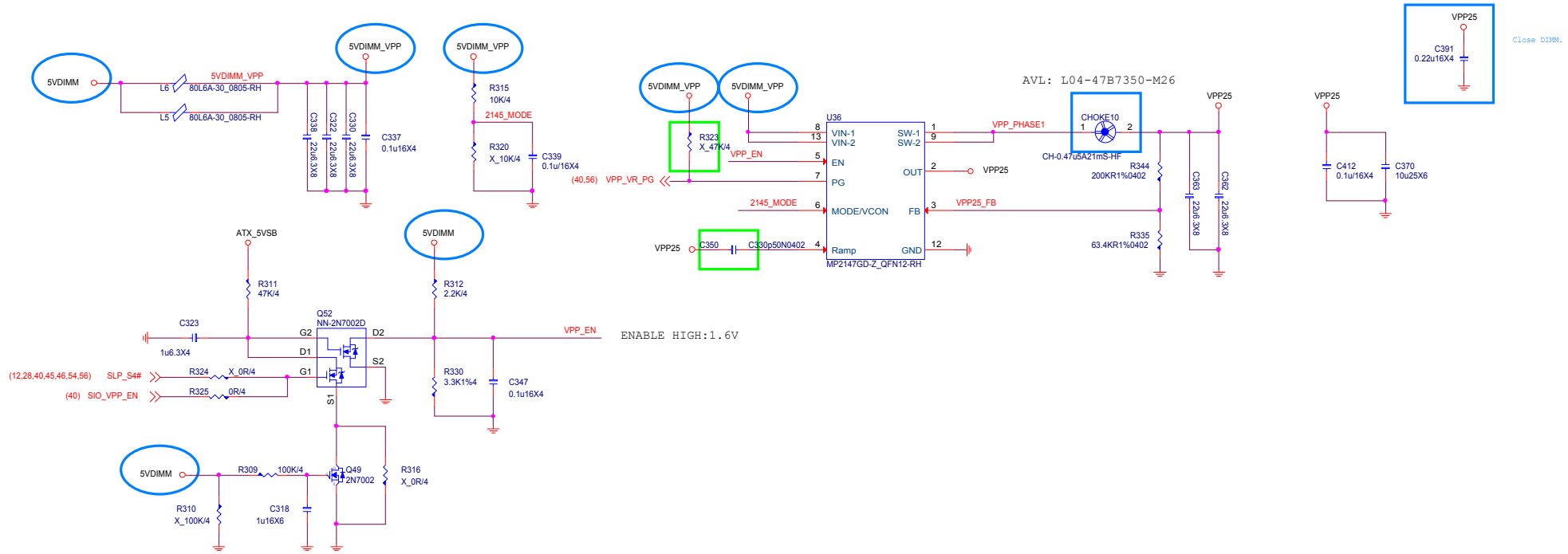
MICRO-STAR INT'L CO.,LTD

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Size Custom	Document Description DDR4 Power-RT8125C	Rev 1.0
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4DIMM :2.24A FOR DDR VPP2.5V

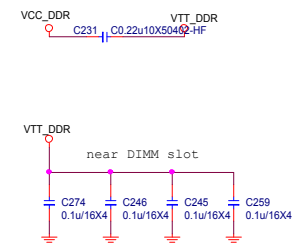
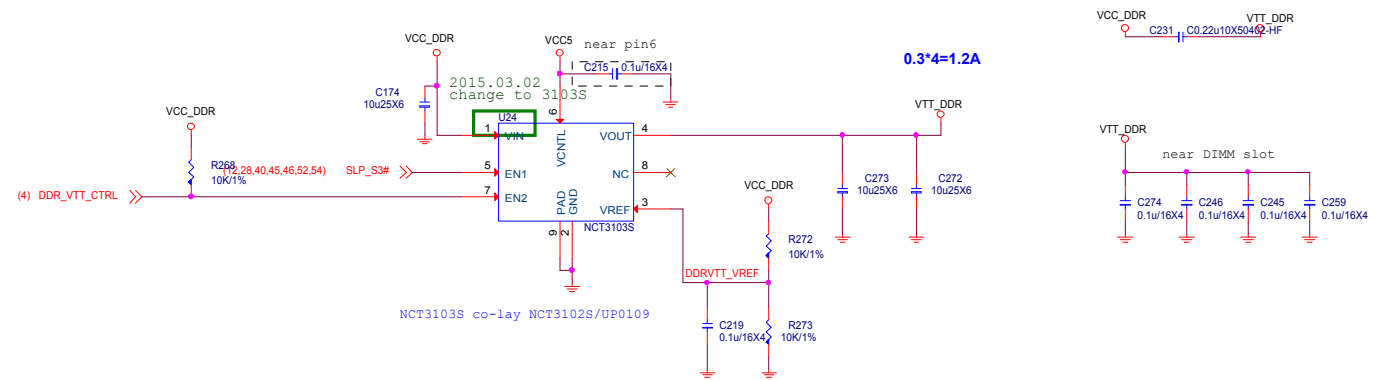
VPP25 Power
2.5V; 2.24A



To make sure VPP EN after 5VDIMM stable

Vinafix.com

DDR VTT Power



MICRO-STAR INT'L CO.,LTD

MS-7B49

Size Custom	Document Description DDR4 Power-VPP25	Rev 1.0
Date: Tuesday, June 27, 2017	Sheet 57 of 69	

PCH 1VSB

1.0V; 11A

$$\begin{aligned} \text{Rocpset} &= 3.48\text{K} \\ \text{OCP} &= \text{Rocpset} * \text{Rdson}(\text{Low side}) / 10\mu\text{A} \\ &= 3.48\text{K} * 4.6\text{mohm} / 10\mu\text{A} \\ &= 16\text{A} \end{aligned}$$

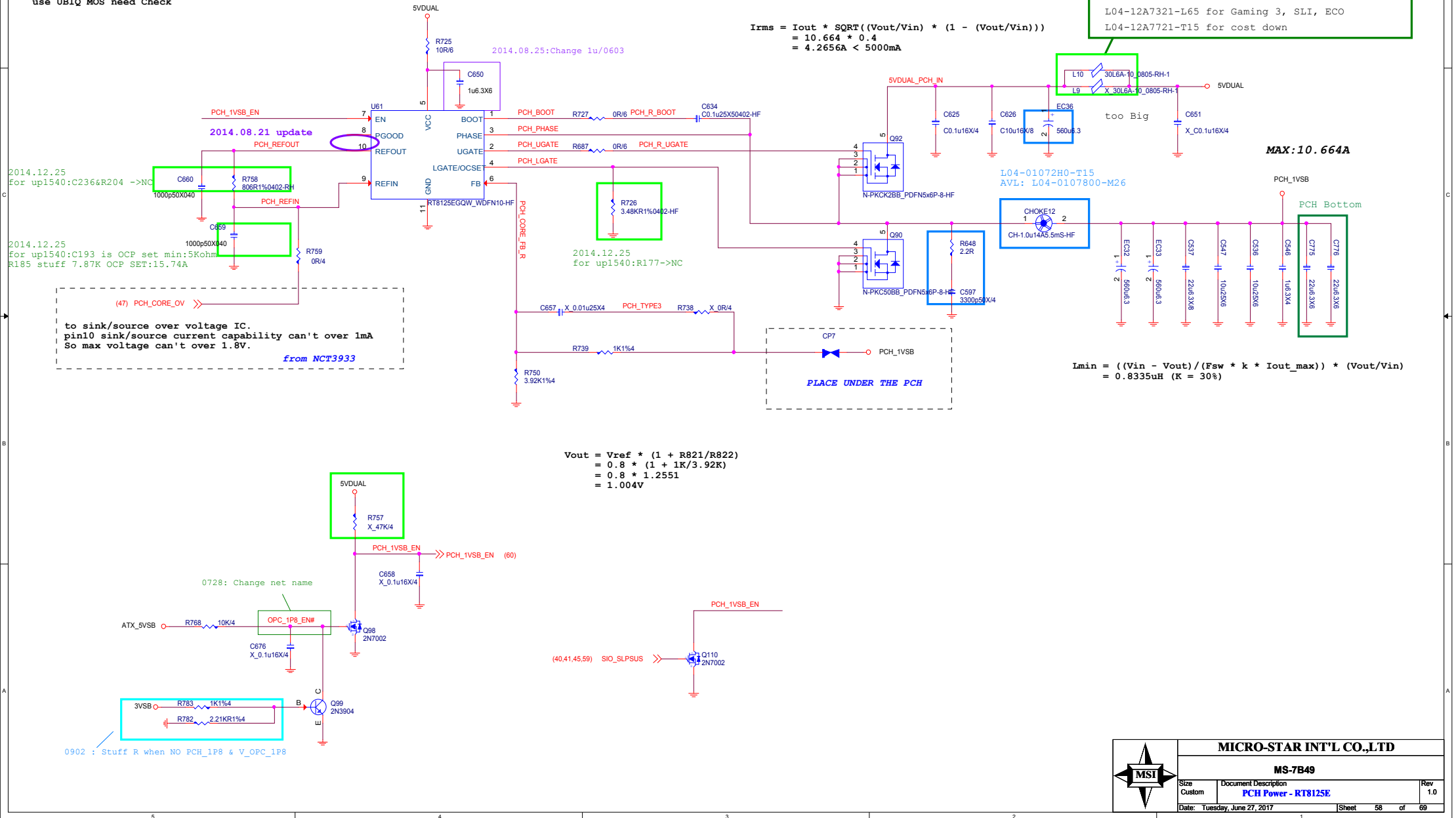
Rocs:7.87K,OCP:
D03-4C05N03-O05 : 15.74A
D03-632BA0C-N03 : 17.1A
use UBIQ MOS need Check

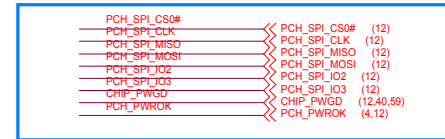
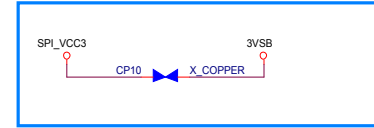
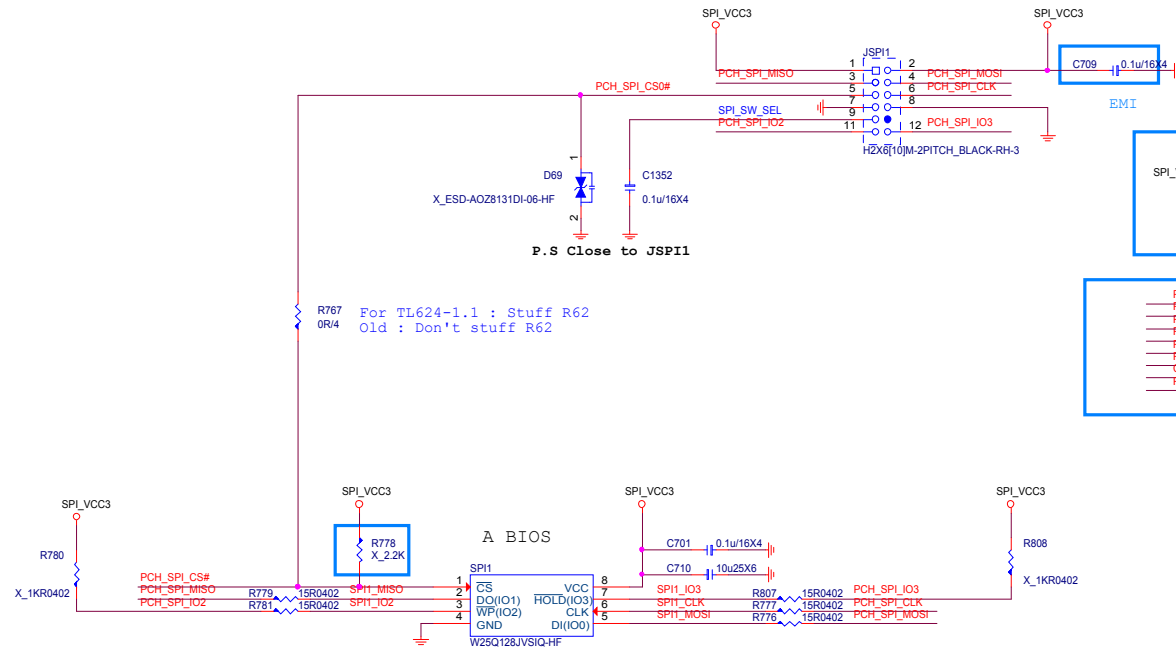
Rdson (low) 4.5V

D03-3116M00-U47 : 3.6 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm

$$\begin{aligned} I_{rms} &= I_{out} * \text{SQRT}((V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))) \\ &= 10.664 * 0.4 \\ &= 4.2656A < 5000mA \end{aligned}$$

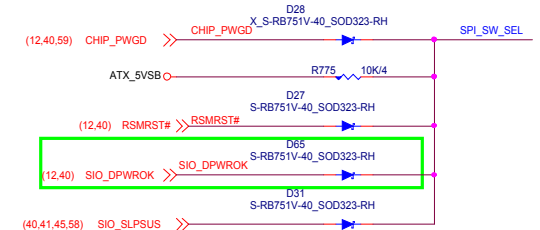
L04-47B7730-T15 for OC, Gaming 10, 9, 7, 5
L04-12A7321-L65 for Gaming 3, SLI, ECO
L04-12A7721-T15 for cost down





Module Stuff CHIP_PWGD,
But PCH_PWROK may ramp up before CHIP_PWGD.

For TL624 1.1



For TL624-1.1
SKYLAKE : Stuff D10/D17/R353
B85/H87 : Stuff D8/D9/R353
Others : Stuff R272



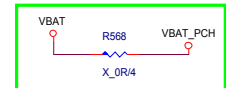
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Size	Document Description	Rev
Custom	SPI ROM	1.0
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20160505

Co-Lay NOT U18 , Stuff R260



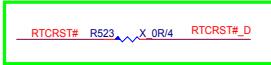
Function 1		
IN		OUT
INPUT1	INPUT2	OUTPUT1
0	1	1
1	0	0
1	1	0
0	0	0

Default

Function 2				
IN		OUT		
INPUT3 & lowswitch EN	INPUT4	OUTPUT2	OUTPUT3	VOUT
0	0	0	1	1
1	0	1	1	0 (discharge)
0	1	1	0	0 (discharge)
1	1	1	0	0 (discharge)

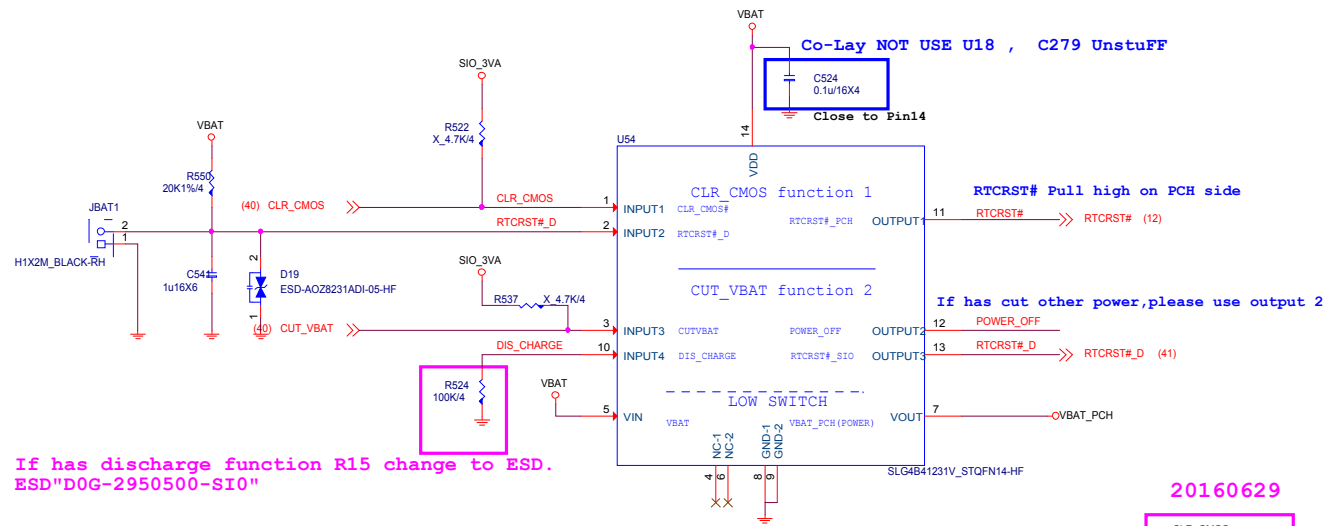
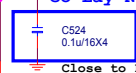
Default

Co-Lay NOT USE U1 , R20 STUFF



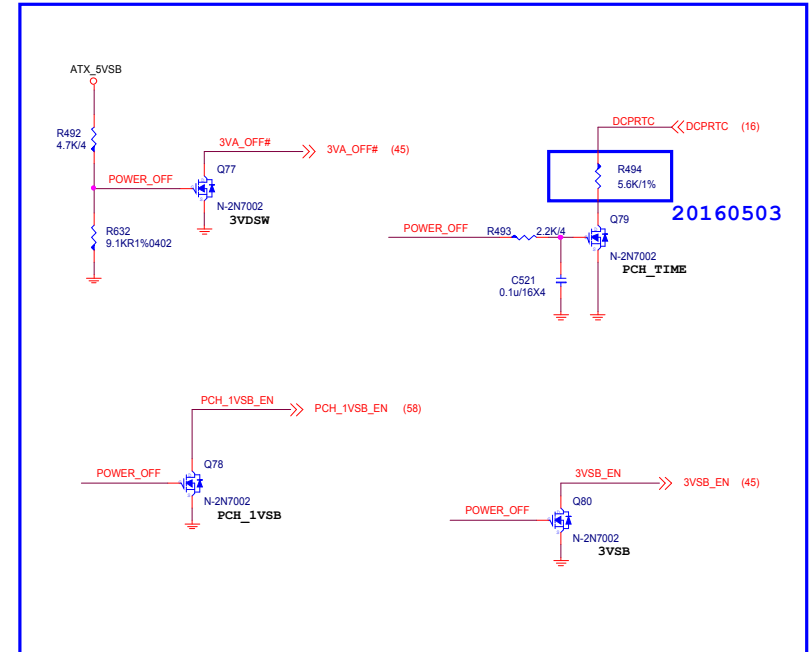
If STUFF R20 Please Check RTCRST# Double Pull High

Co-Lay NOT USE U18 , C279 Unstuff



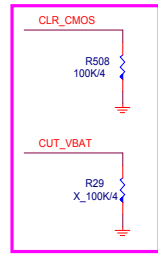
If has discharge function R15 change to ESD. ESD"D0G-2950500-SI0"

Co-Lay NOT USE U1 , ALL UNSTUFF



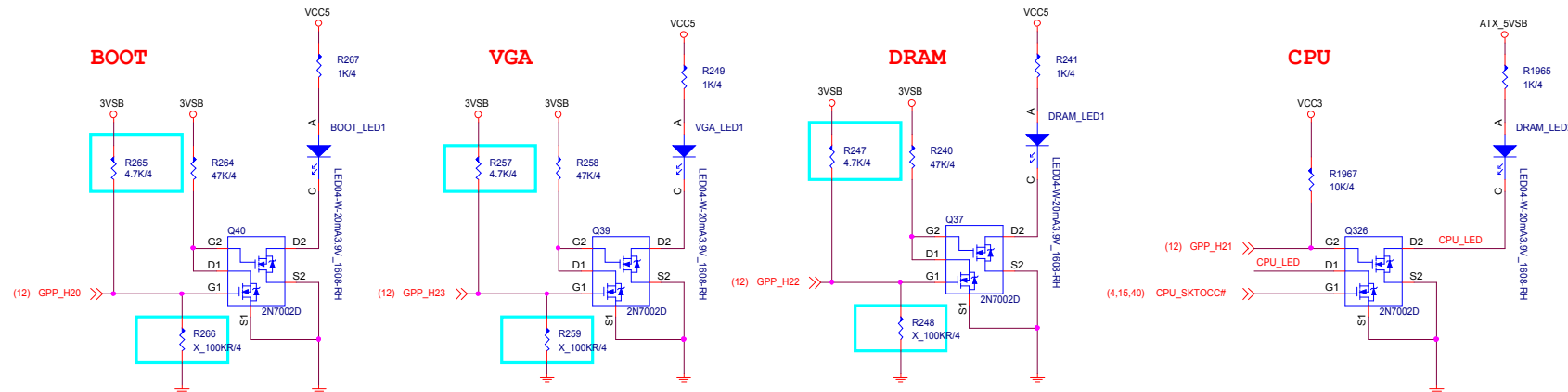
20160503

20160629



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EZ Debug

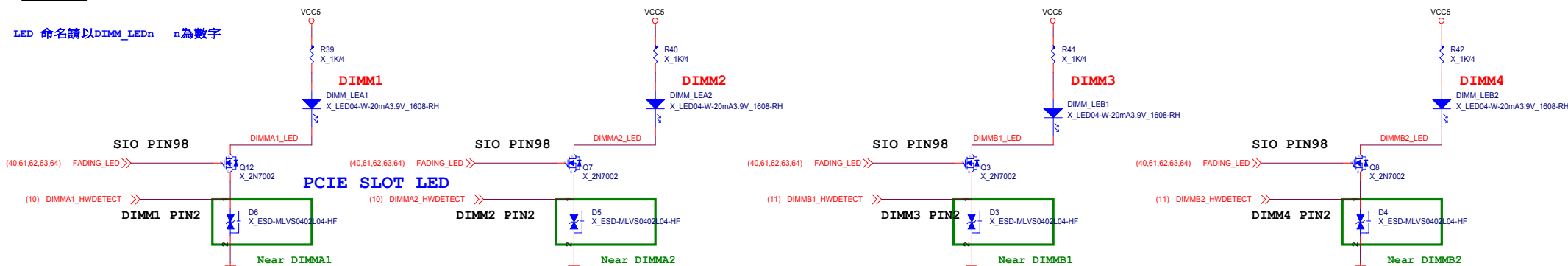


白 M:DOC-040T200-H91
S:DOC-040S200-E07

TOP LED
紅 M:DOC-040P100-H91
S:DOC-040S500-E07

DIMM

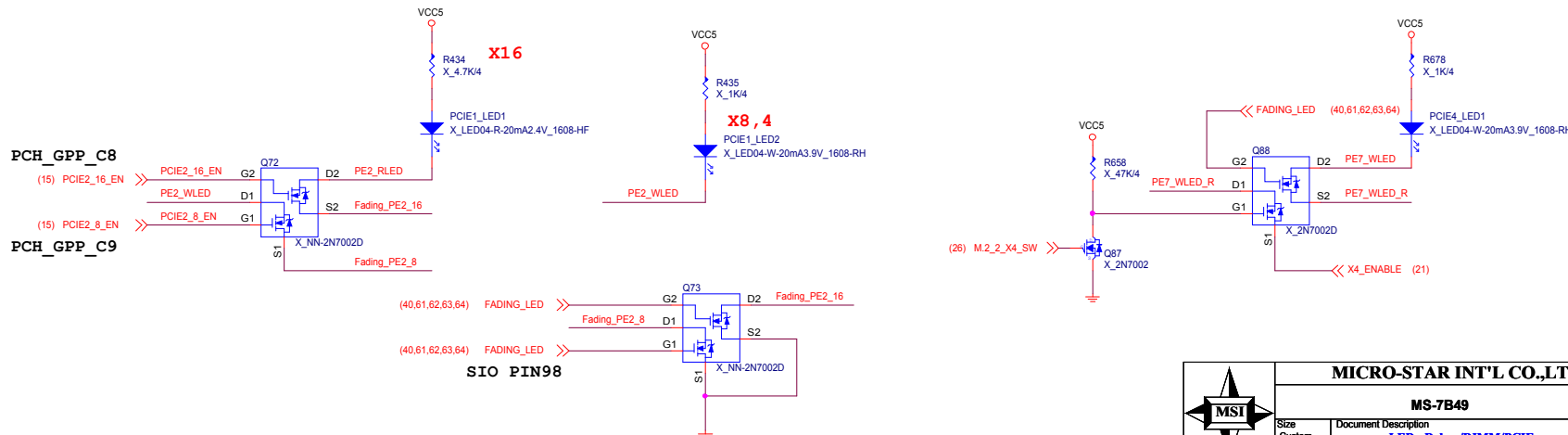
LED 命名請以DIMM_LEDn n為數字



PCIE

PCIE SLOT LED 命名請以PCIE_LEDn n為數字

GPIO LED	GPP_C8	GPP_C9
亮	GPO PO HIGH	GPO PO HIGH
滅	GPI (default LOW)	GPI (default LOW)

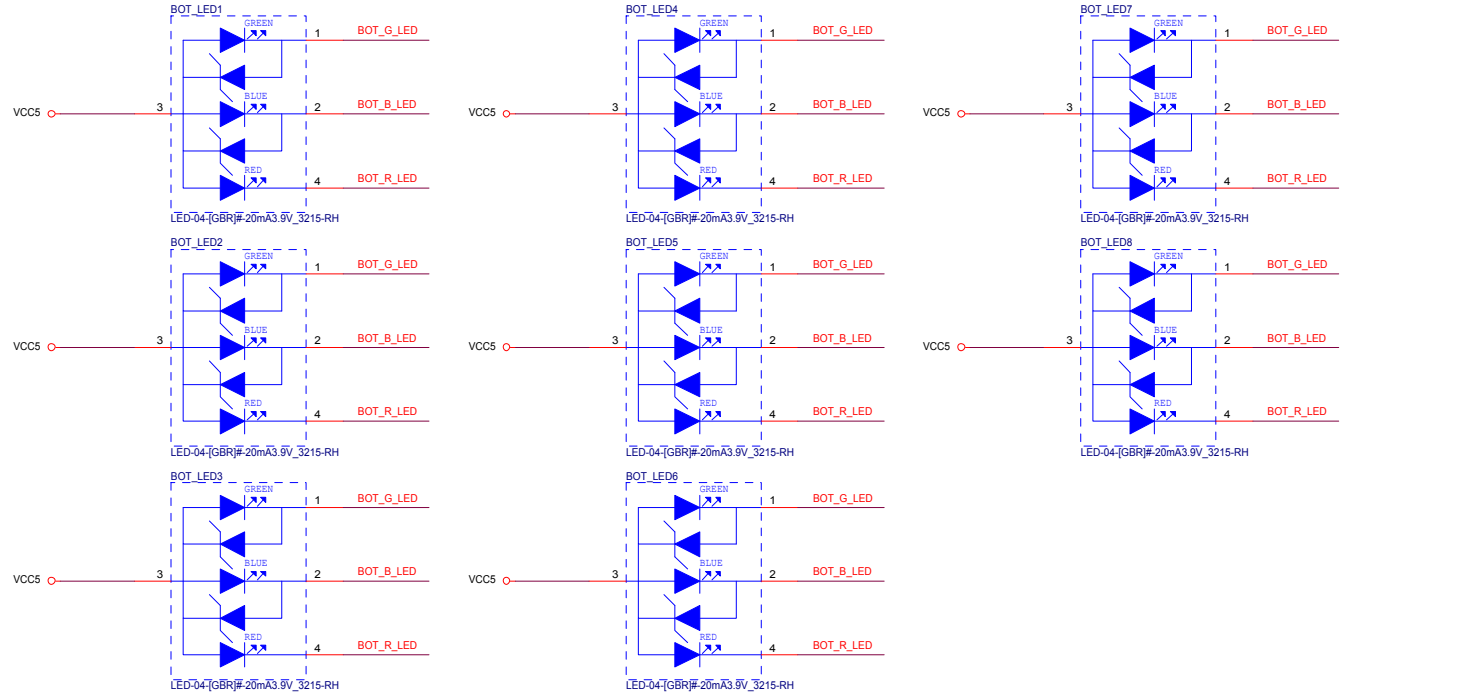


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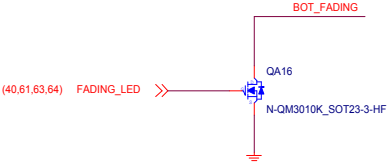
BOTTOM LED



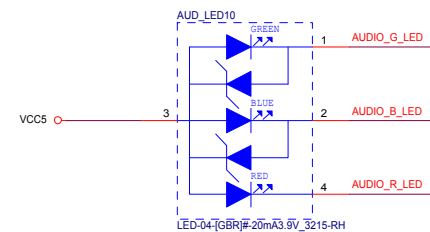
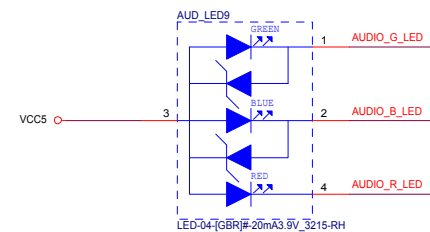
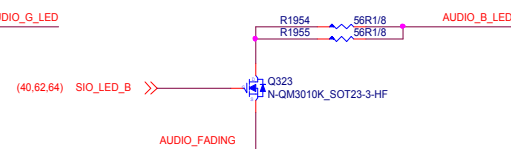
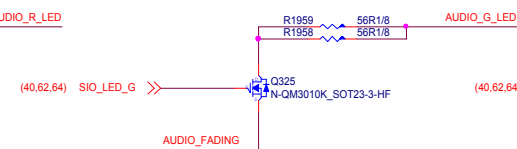
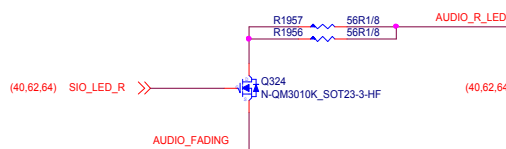
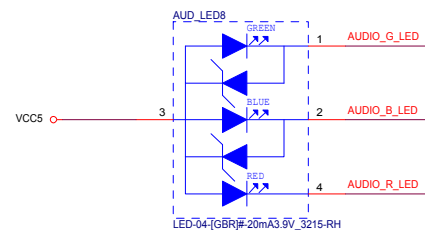
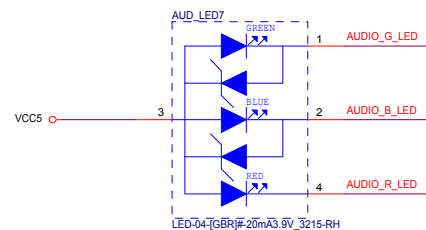
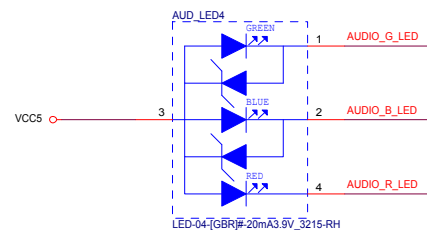
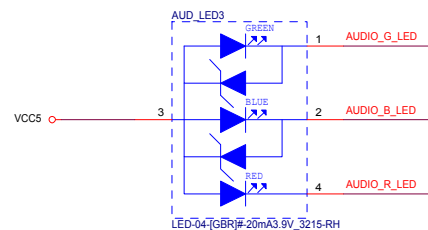
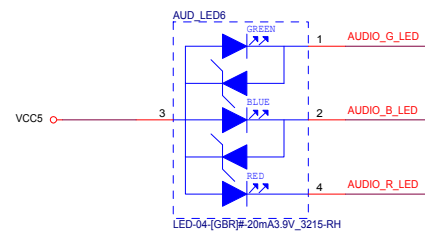
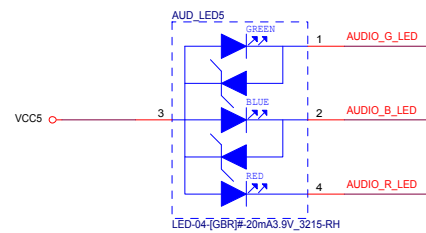
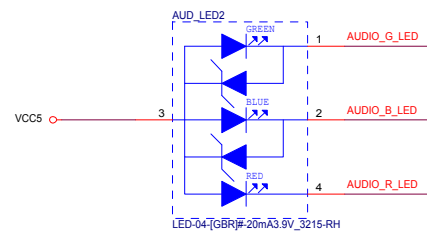
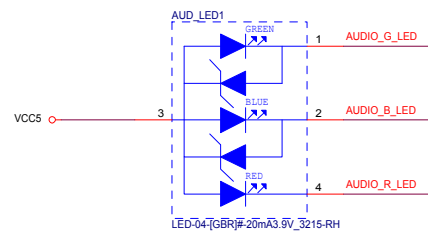
Vf=1.7 V~2.3V
5.05V-1.9V/27.3=0.115A
0.115A*0.115A*27.3=0.36W
PS:實際量測LED Vf=1.9v

Vf=2.7 V~3.45V
5.05V-2.8V/27.3=0.0824A
0.0824A*0.0824A*27.3=0.185W
PS:實際量測LED Vf=2.8v

Vf=2.7 V~3.45V
5.05V-2.9V/27.3=0.0787A
0.0787A*0.0787A*27.3=0.169W
PS:實際量測LED Vf=2.9v



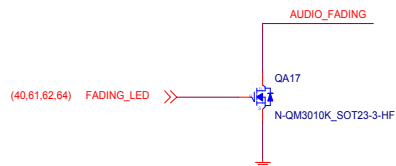
AUDIO LED



Vf=1.7 V~2.3V
 $5.05V - 1.9V / 27.3 = 0.115A$
 $0.115A \times 0.115A \times 27.3 = 0.36W$
 PS:實際量測LED Vf=1.9v

Vf=2.7 V~3.45V
 $5.05V - 2.8V / 27.3 = 0.0824A$
 $0.0824A * 0.0824A * 27.3 = 0.185W$
 PS:實際量測LED Vf=2.8v

Vf=2.7 V~3.45V
 $5.05V - 2.9V / 27.3 = 0.0787A$
 $0.0787A * 0.0787A * 27.3 = 0.169W$
 PS:實際量測LED Vf=2.9v



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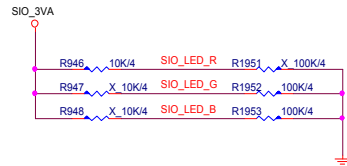
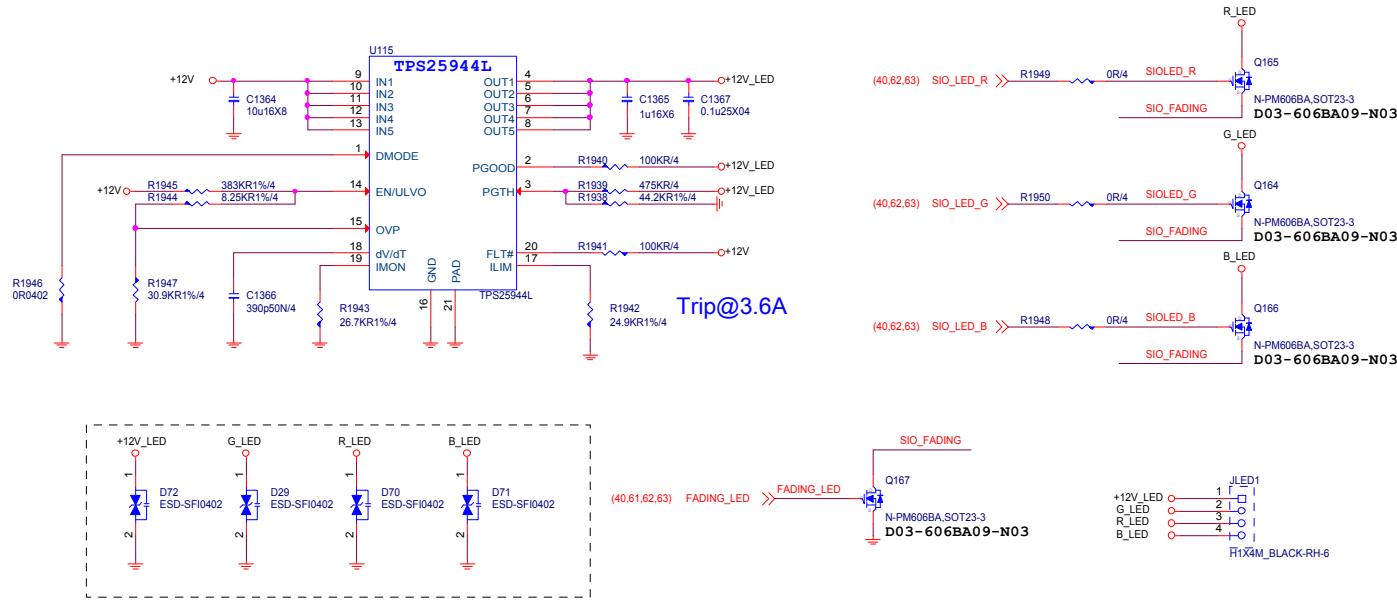


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LED Control by SIO



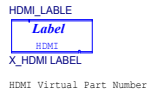
Color	SIO_LED_R	SIO_LED_G	SIO_LED_B
RED	1	0	0
GREEN	0	1	0
BLUE	0	0	1
WHITE	1	1	1

PCB



PD0-07B4910-G37, 精成-深圳, 28, 寶安恩斯邁廠 (MSIS)
PD0-07B4910-E48, 競華, 24, 寶安恩斯邁廠 (MSIS)

CPU Socket



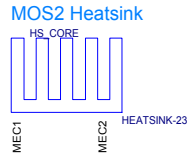
Battery



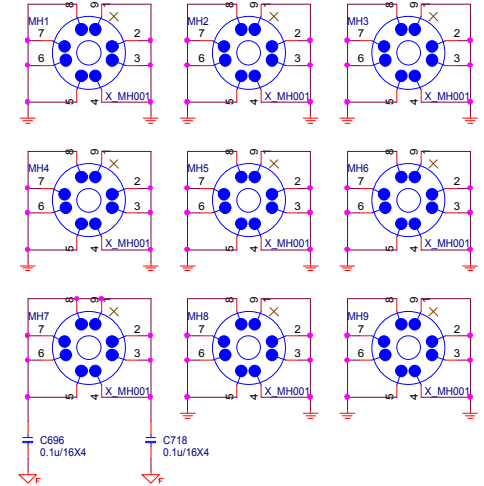
BIOS Label



MOS1 Heatsink



Mounting Holes



Simulation



Test point



Optical Fiducial Marks-120

